SEEQ

8005
Advanced Ethernet
## Data Link Controller (AEDLC™)

June 1991

Features

- **Conforms to IEEE 802.3 Standard**
  - Ethernet (10BASE-5) Cheapernet (10BASE-2) and Twisted Pair (10BASE-T)
- **Recognizes One to Six Selectable Station or Multicast Addresses**
- **Advanced Error Detection/Handling:**
  - Automatic Re-Transmit after collision
  - Auto discard of bad packets
- **Software Selection of 2 Byte or 6 Byte Station Addresses**
- **Optional Preamble and Cyclic Redundancy Code (CRC) Generation/Checking**
- **Manages 64K Bytes of Local Packet Buffer**
  - Connects to RAS/CAS/Data/Control of 64K x 4 Dynamic RAMS
  - Automatic DRAM Refresh
  - Automatic Posting of Status Packet in Buffer

- **Flexible System Bus Interface**
  - 8 or 16 Bit Data Transfers with Byte Swap Capability
  - Programmable DMA Burst Length
  - Selectable for Intel or Motorola Compatible Bus Signals
- **Connects Directly to 8020 Manchester Code Converter (MCC™)**
- **Uses Fewer Support Chips**
  - Lower System Costs
  - Higher Reliability
- **68 Pin Surface Mount Plastic Leaded Chip Carrier Package**

Pin Configuration
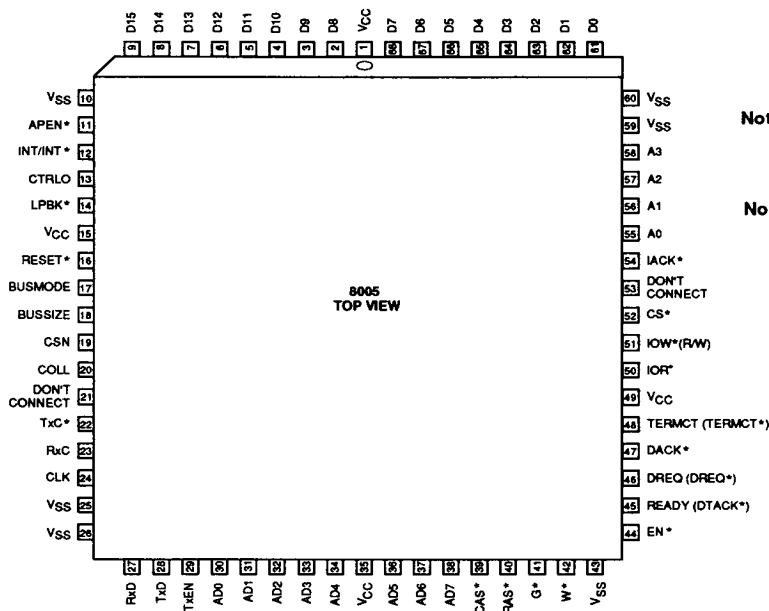
Note: Signal names in paranthesis apply when BUSMODE = 0.

Note: Do not connect any signals to pins 21 and 53 to allow for future compatibility.

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MD400031/E   19

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Pin Description

(An asterisk after a signal name signifies an active low signal)

D0-D15: A 16 bit bidirectional system data bus. If BUS-SIZE = 0, the bus is configured as 8 bits and D8-D15 are not used for data transfer. Byte order for local buffer data transfers on a 16 bit bus is software configured. D8-D15 are used to provide address information to the optional external address PROM in both 8 and 16 bit modes.

EN*: An output which can be used to control the three-state control pin of external bi-directional drivers such as the 74LS245.

APEN*: Active low address PROM enable output.

IOW*(R/W): If BUSMODE = 1, this input defines the current bus cycle as a write. If BUSMODE = 0, this input defines the bus cycle as a read if a 1 or a write if a 0.

IOR*: If BUSMODE = 1, this input defines the current bus cycle as a read. If BUSMODE = 0, this input is not used.

CS*: The chip select input, used to access internal registers and the packet buffer.

A0-A3: Address select inputs used to select internal registers for reading or writing. A0 is not used in 16-bit mode.

DACK*: An input used to acknowledge granting of the system bus for external DMA transfers. When DREQ is active, DACK* functions as a chip select for reads and writes.

DREQ(DREQ*): An output to an external DMA controller used to signal that a DMA request is being made. This signal is high active when BUSMODE = 1, low active when BUSMODE = 0. A three-state output.

TERMCT(TERMCT*): An input which signals that the last byte or word of a DMA access is on the bus. When BUSMODE = 1, this input is high active; when BUSMODE = 0, it is low active.

READY(DTACK*): A three-state output. When BUSMODE = 1, this output functions as a READY pin (Intel compatible); when BUSMODE = 0, this output is DTACK* (Motorola compatible).

INT/INT*: When BUSMODE = 1, this is a high active interrupt output; when BUSMODE = 0 this output is low active.

IACK*: Active low interrupt acknowledge input. When this input is asserted and INT is also asserted, the contents of the Interrupt Vector register are placed on D0-D7.

RESET*: The low active reset input. Asserting RESET* clears all configuration and pointer to 00. Following reset, a wait of 4 µs is necessary before accessing the part.

BUSMODE: An input which selects Intel-compatible bus signals when high or Motorola-compatible bus signals when low.

BUSSIZE: An input that selects the 8-bit system bus when low or 16-bit system bus when high.

AD0-AD7: A multiplexed address and data bus used to provide row and column address and read/write data to the packet buffer dynamic RAM.

RAS*: Row Address Strobe to the packet buffer memory.

CAS*: Column Address Strobe to the packet buffer memory. Page mode addressing is used when possible to speed access to the buffer.

W*: An output to the dynamic RAM buffer that indicates the current cycle is a write.

G*: An output to the dynamic RAM buffer that enables read data onto the AD bus.

TxEN: An output to the Manchester Code Converter that indicates a transmission is in progress.

TxC*: An input from the Manchester Code Converter that is used to synchronize transmitted data.

TxD: The transmit data output to the Manchester Code Converter.

RxC: An input from the Manchester Code Converter used to synchronize received data.

RxD: The receive data input from the Manchester Code Converter.

COLL: The collision input from the Manchester Code Converter.

CSN: The carrier sense input from the Manchester Code Converter.

CTRLO: Control/Output, a general purpose control pin, level follows bit 12 of Configuration Register #2.

LPBK*: The loopback control output.

CLK: The master 20 MHz input clock.

Block Diagram Description

The 8005 AEDLC has three major blocks: the Ethernet Data Link Controller, Buffer Controller and Bus Interface. (See 8005 Internal Block Diagram).

The 8005 supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, CRC generation/stripping, transmission deferral, collision handling and address recognition of up to 6 station addresses as well as multicast/broadcast addresses. CTRLO and LPBK* are general

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purpose outputs that can be used to control, for example, the loopback function of the 8020/8023A Manchester Code Converter (MCC). For non-IEEE 802.3 applications such as serial backplane buses, support is also provided for 2 byte address recognition, reduced slot time and reduced preamble length.

The Buffer Controller provides management for a 64K byte local packet buffer consisting of two 64K x 4 dynamic RAMS. This block provides arbitration and control for four different memory ports: the 8005 Transmitter, for network transmit packets; the 8005 Receiver, for received frames; the Bus Interface, for system data and control; and an internal DRAM refresh generator. To minimize pin count, dynamic RAM addresses and data are time multiplexed on a single 8 bit bus. A control line and an 8 bit address is also provided to permit reading from a locally attached

EEPROM or PROM. This permits configuring a P.C. board with its station address(es) and configuration data independent of the network layer software used.

The Buffer Controller interfaces to the system bus and provides access to internal configuration/status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called DMA FIFO. This permits high speed data transfers to occur even when the Buffer Controller is busy servicing the Transmitter or Receiver or refreshing the DRAM. Both 8 and 16 bit transfers are supported, and byte ordering on a 16 bit bus is under software control. The 8005 supports both Intel-compatible and Motorola-compatible buses.
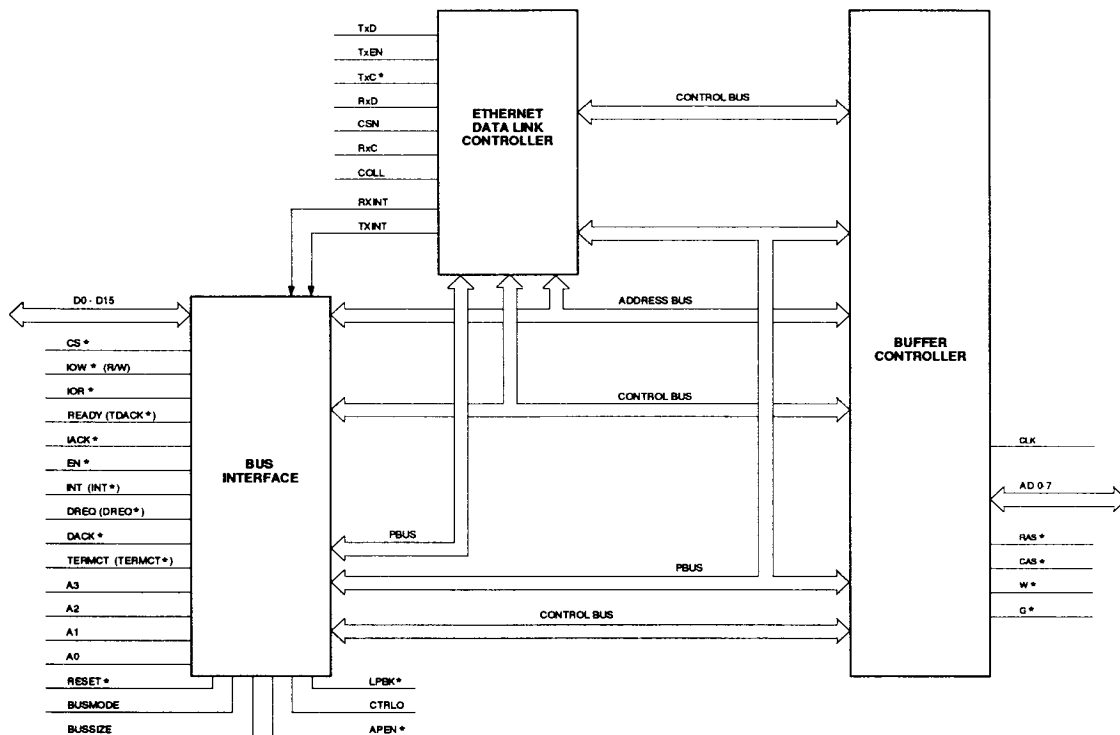
8005 Internal Block Diagram

The 8005 Interconnect Diagram

The system interconnect diagram shows the 8005 in a typical system configuration, connecting to the LAN via an 8020 Manchester Code Converter. The Attachment Unit Interface connects to an Ethernet (10BASE-5); Cheapernet (10BASE-2); or a twisted pair (10BASE-T) network.

Separate TMS 4464-120 64K DRAMs store received packets, or packets waiting for transmission. AD_0-AD_7 address both RAMs. Data is exchanged on the AD leads, DQ_0 - DQ_3 to one RAM, and DQ_4 - DQ_7 to the other RAM.

The System Bus exchanges data with the Buffer Controller in the 8005. Two bi-directional data buffers (74LS45) interface 16-bit data, only one buffer is used for 8-bit data. The 2804 PROM stores the node address. The 8005 has six 6-byte address fields.

Buffer Management

The Buffer Controller manages a 64K byte packet buffer into which packets that are received are temporarily stored until the system either reads or disposes of them and packets placed there by the system are held for transmission over the link. The buffer is logically divided into separate receive and transmit areas of selectable size. The transmit area always originates at address 0. Each packet in the buffer is prefixed by a header of 4 bytes that contains command and status information and a 16 bit pointer to the start of the next packet in the buffer.

To transmit packets, the system loads one or more packets of data, complete with header information, into the transmit area of the buffer and commands the 8005 to begin transmission, starting from the address contained in the Transmit Pointer. When transmission is complete, the 8005 updates the status byte in the header and interrupts the system if so programmed. The Transmit Pointer automatically wraps to location 0 when the Transmit End Area is reached.

The Buffer Controller manages the buffer area as a circular buffer with automatic wraparound. As data is received from the 8005 it is stored in the buffer beginning at the location specified by the Receive Pointer. The Receive Pointer will wrap from FF,FF to Transmit End Area + 1,00. For example, if TEA = 80 the Receive Pointer wraps to 81,00. If the Receive Pointer reaches Receive End Area,00 an overflow has occurred. The Receiver is turned off and an interrupt is issued. Restarting the Receiver is accomplished by freeing up buffer space and turning the Receiver back on.

Transmit Packet Format

Each Packet to be transmitted consists of a four byte header and up to 65,532 bytes of data which are placed into the local buffer via the Bus Interface. The header contains the following information in the indicated order:

1. Most significant byte of the address of the next packet header.

2. Least significant byte of the address of the next packet header.

3. A transmit command byte.

4. A transmit status byte which should be initialized to zero by the system and will contain status for this packet when transmission is complete.

Bytes 1 and 2, called the Next Packet Pointer, point to the location immediately following the last byte of the packet, which is the first byte of the next packet header, if it exists. In 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used. Byte 1 is the more significant byte.

Byte 3 is the Transmit Command byte. It contains information to guide the controller in processing the packet associated with this block.

> **Bit 0: Xmit Babble Int. Enable.** The 8005 will transmit packets as large as the Transmit buffer can hold but will abort packets and interrupt if this bit is set to a one. This condition is caused by an attempt to transmit a packet larger than the allowed 1514 bytes, excluding preamble and CRC. If babble occurs with bit 0-Xmit Babble Int. Enable set to a 1 on byte 3-the Transmit Command byte, the Transmitter will abort transmission and turn itself off. When the bit is set to 0, no interrupt is generated, and the Transmitter is not turned off, but a status bit is set in the Status Header.

> **Bit 1: Xmit Collision Interrupt Enable.** When set to a one, a Transmit Interrupt will be generated if a collision occurs during a transmit attempt.

> **Bit 2: 16 Collisions Enable.** When set to a one, a Transmit Interrupt will be generated if 16 collisions occur during a transmit attempt, and the transmitter will be turned off. When set to 0 no interrupt is generated, and the transmitter will not be turned off, but a status bit is set in the Status Header.

> **Bit 3: Xmit Success Interrupt Enable.** When set to a one, a Transmit Interrupt will be generated if the transmission is successful, that is, fewer than 16 collisions occurred.

Bit 4: *Not used.*

Bit 5: Data Follows: *If this bit is cleared to a zero, the transmitter will process this header as a pointer only, with no data associated with it. This provides a means to redirect the Transmit Pointer.*

Bit 6: Chain Continue. *If set to a one, there are more headers in the chain to be processed. If this bit is a zero, the header is the last one in the chain.*

Bit 7: Xmit/Receive. *If this bit is a one, the current header is for a packet to be transmitted. If this bit is a*

zero, the packet header will be processed as a header only and no data follows (bit 5).

Byte 4 *is the Transmit Status byte, which is written by the Buffer Controller upon conclusion of each packet transmission or retransmission attempt. It provides for reporting of both normal and error termination conditions of each transmission.*

Bit 0: Xmit Babble. *If set to a one, transmit babble occurred during the transmission attempt. This is caused by an attempt to transmit a packet larger than*
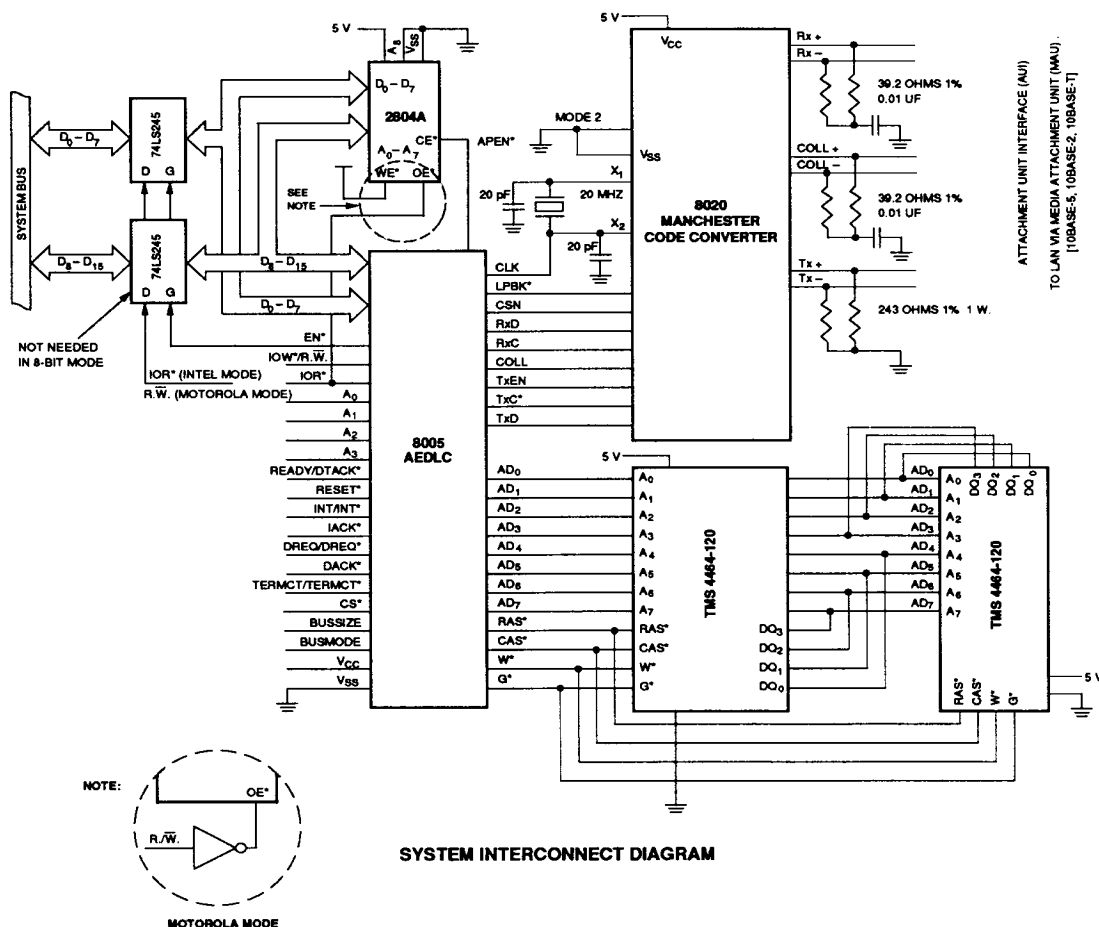
SYSTEM INTERCONNECT DIAGRAM

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the allowed 1514 bytes, excluding preamble and CRC. If babble occurs with bit 0-Xmit Babble Int. Enable set to a 1 on byte 3, the Transmit Command byte, the transmitter will abort transmission and turn itself off.

Bit 1: Xmit Collision. If set to a one, a collision occurred during the transmission attempt.

Bit 2: 16 Collisions. If set to 1, 16 collisions occurred during the transmission attempt.

Bit 3, 4, 5 and 6: Reserved.

Bit 7: Done. If set to a one, the controller has completed all processing of the packet associated with this header (either the packet has been sent successfully or 16 collisions occurred) and there is now valid status in the Status byte.

The data field follows the fourth byte.

Receive Packet Format

Each Packet received is preceded by a four byte header and is placed into the local buffer via the Buffer Controller. The header contains the following information in the indicated order:

1. Most significant byte of the address of the next packet header.

2. Least significant byte of the address of the next packet header.

3. Header Status byte.

4. Packet Status byte .

Bytes 1 and 2, called the Next Packet Pointer, point to the first byte of the next receive packet header. The next packet header starts immediately after the end of the current packet. The packet length is equal to the difference between the starting addresses of the two packet headers minus 4. If the value of the Next Packet Pointer is less than the current one, the pointer has wrapped around from the end of the buffer to the Receive Start Area (the Receive Start Area equals the Transmit End Area address + 1). When in 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used.

The third byte of the header contains header information associated with this packet.

Bits 0 through 5: Not Used.

Bit 6: Chain Continue. If this bit is set to a one, there are more packets in this chain to be processed. If this bit is a zero, this packets is the last one in the chain and this header space will be used for the next packet that is received.

Bit 7: Xmit/Receive. This bit is always set to 0 by the controller to indicate a receive packet header.

The fourth byte of the header, called the Packet Status byte, contains status information resulting from processing the packet associated with this block.

Bit 0: Oversize Packet. If this bit is a one, the packet was larger than 1514 bytes, excluding the Preamble and CRC fields.

Bit 1: CRC Error. If this bit is a one, a CRC Error occurred in this frame. CRC status is captured on byte boundaries, so that 7 or less dribble bits will not cause a CRC error.

Bit 2: Dribble Error. Packets are integral multiples of octets (bytes). If this bit is a one, the received packet did not end on an octet (byte) boundary.

Bit 3: Short Packet. If this bit is a one, the packet contained less than 64 bytes including CRC. Short packets are properly received as long as they are at least 6 bytes long; packets with less than 6 bytes will only be received if the match mode bits in Configuration Register #1 specify promiscuous mode, multicast/ broadcast is selected and the first bit of the destination address is a 1, or the 2-byte address mode has been selected.

Bits 4 , 5 and 6: Not used.

Bit 7: Done. If this bit is a one, the controller has completed all processing of this packet and there are now valid pointers and status in this header. The user may now move this packet out of the local buffer, if desired, and reuse this buffer space.

The data field follows this byte, unless this is a header only packet.

Registers

There are nine directly accessible 16 bit registers in the 8005, one of which is used as a "window" into indirectly accessed registers as well as the local buffer memory. Access is controlled by chip select, I/O read, I/O write and four address inputs, A0-A3. The following description assumes a 16 bit wide system interface; as such, the low order address input, A0, is shown as "X," a don't care. In 8 bit mode, input pin A0 selects bits 0 through 7 of the register when a zero, and bits 8 through 15 when a one. Note that the byte swap bit does not affect the byte order of these registers.

All "not used" bits should be set to 0 to maintain future compatibility. When read, "not used" bits read as '1'.

Command Register, A3-0 = 000X (Write only)

Bit 0: DMA Interrupt Enable. When set to a 1, completion of a DMA operation, as signaled by Terminal Count, will generate an interrupt.

Bit 1: Rx Interrupt Enable. When set to a 1, this bit enables interrupts whenever a packet becomes available in the packet buffer.

Bit 2: Tx Interrupt Enable. When set to a 1, this bit enables interrupts for completion of transmit operations. See the Transmit Header Command byte description for conditions that can cause an interrupt.

Bit 3: Buffer Window Interrupt Enable. Setting this bit to a one enables interrupts for Buffer Window register reads from the packet buffer.

Bit 4: DMA Interrupt Acknowledge. Setting this bit to a one causes a pending DMA interrupt to be cleared.

Bit 5: Rx Interrupt Acknowledge. Setting this bit to a one causes a pending Receive interrupt to be cleared.

Bit 6: Tx Interrupt Acknowledge. Setting this bit to a one causes a pending Transmit interrupt to be cleared.

Bit 7: Buffer Window Interrupt Acknowledge. Setting this bit to a one causes a pending Buffer Window interrupt to be cleared.

Bit 8: Set DMA On. Setting this bit to a one enables the DMA request logic. If the DMA FIFO is set to the read direction, a DMA Request will be asserted when the DMA FIFO has enough bytes to satisfy the burst size. If the DMA FIFO is in the write direction the DMA Request will be asserted immediately. Clearing this bit has no effect. Setting this bit with bit 11 set will force a DMA Interrupt, provided the DMA Interrupt Enable bit is set, which permits testing the interrupt without actually performing DMA operations.

Bit 9: Set Rx On. Setting this bit to a one enables the Receiver. Clearing this bit to a 0 has no effect. Setting this bit with bit 12 set will force an interrupt, provided the Receive Interrupt Enable bit is set, which permits testing the interrupt without receiving packet data.

Bit 10: Set Tx On. Setting this bit to a 1 enables the Transmitter. The Buffer Controller will read the header information pointed to by the Transmit pointer and process the packet accordingly (see transmit packet header description). The conditions for interrupting upon completing packet processing are specified in the Transmit Header Command byte, which is stored in the buffer memory. Setting this bit with bit 13 set will force a transmit interrupt for test purposes.

Bit 11: Set DMA Off. Setting this bit to a one disables the DMA Request logic.

Bit 12: Set Rx Off. Setting this bit to a one disables the receive logic. If the 8005 is actively receiving a packet when bit 12 is set, the Receiver will be disabled after completing reception of the packet. Bit 9 Rx On will be '1' until the receiver is disabled. If Bit 1 is set to a 1, Rx interrupt will also be generated.

Bit 13: Set Tx Off. Setting this bit to a one disables the transmitter. If a packet is being transmitted when this bit is set, the packet will be aborted.

Bit 14: FIFO Read. When set to a one, the DMA FIFO direction is set to read from the packet buffer. The FIFO direction should not be changed from a write to a read until it is empty (see FIFO status bits).

Bit 15: FIFO Write. When set to a one, the DMA FIFO direction is set to write to the packet buffer. Changing the DMA FIFO direction clears the DMA FIFO.

Status Register, A3-0=000X (Read only)

Bit 0: DMA Interrupt Enable. When set, this bit indicates that interrupts are enabled for terminal count during a DMA operation.

Bit 1: Rx Interrupt Enable. When set, this bit indicates that interrupts are enabled for receive events.

Bit 2: Tx Interrupt Enable. When set, this bit indicates that interrupts are enabled for transmit events.

Bit 3: Buffer Window Interrupt Enable. When set, this bit indicates that interrupts are enabled for Buffer Window reads from the packet buffer.

Bit 4: DMA Interrupt. When set, this bit indicates that DMA has been terminated, either due to terminal count or the DMA On bit being written off. If the associated Interrupt Enable bit is set, an interrupt will also be asserted.

Bit 5: Rx Interrupt. When set, this bit indicates that a Receive packet chain is available. If the associated Interrupt Enable bit is set, an interrupt is also asserted.

Bit 6: Tx Interrupt. When set, this bit indicates that a Transmit interrupt condition has occurred. The following are valid Tx Interrupt conditions: Xmit Babble, Xmit Collisions, Xmit 16 Collisions and Xmit Success. If the Tx Interrupt enable bit is set, an interrupt is also asserted.

Bit 7: Buffer Window Interrupt. When set, this bit indicates that data has been read from the local buffer into the DMA FIFO and is ready to be read via the Bus Interface. If the associated interrupt enable bit has been set, an interrupt is asserted.

Bit 8: DMA On. When set, this bit indicates that the DMA logic is enabled. When Terminal Count is as-

serted during a DMA transfer, this bit will be reset to indicate that the DMA activity has been completed. When reset, this bit three-states the DREQ pin.

Bit 9: Rx On. When set, this bit indicates that the Receiver is enabled. This bit remains set during active reception of a packet and turns 'off' at the end of reception if bit 12 Rx off is set.

Bit 10: Tx On. When set, this bit indicates that the Transmitter is enabled.

Bits 11 & 12: Not used.

Bit 13: DMA FIFO Full. When set, this bit indicates that the DMA FIFO is full.

Bit 14: DMA FIFO Empty. When set, this bit indicates that the DMA FIFO is empty.

Bit 15: FIFO Direction. When set, this bit indicates that the DMA FIFO is in the read direction; when cleared, it indicates that the DMA FIFO is in the write direction. After hardware or software reset, this bit is cleared.

Configuration Register 1, A3-0=001X

Bits 0-3: Buffer Code. These four bits are the Buffer Window Code bits, which determine the source of Buffer Window register reads and the destination of buffer window register writes. Buffer code bits 3-0 should be set to '1000' by pointing to local buffer memory before turning FIFO to read direction to perform reads.

Buffer Code Selection Table

Buffer Code Bits				Buffer Window Reg. Contents
3	2	1	0	
0	0	0	0	Station addr. reg. 0
0	0	0	1	Station addr. reg. 1
0	0	1	0	Station addr. reg. 2
0	0	1	1	Station addr. reg. 3
0	1	0	0	Station addr. reg. 4
0	1	0	1	Station addr. reg. 5
0	1	1	0	Address PROM
0	1	1	1	Transmit end area
1	0	0	0	Local buffer memory
1	0	0	1	Interrupt vector
1	0	1	X	Reserved — do not use
1	1	X	X	Reserved — do not use

Bits 4-5: DmaBurstInterval. These two bits specify the interval between DMA requests.

If configured for continous mode, the DMA request will persist until Terminal Count is asserted.

5	4	Burst Interval
0	0	Continuous
0	1	800 nanoseconds
1	0	1600 nanoseconds
1	1	3200 nanoseconds

DMA Burst Size Selection

Bits 6-7: DmaBurstSize. These two bits specify the DMA Burst Transfer count.

7	6	# of DMA Tranfers/Burst
0	0	1
0	1	4
1	0	8
1	1	16 (Illegal in word mode)

Bits 8-13: These six bits select which of the station address register sets (each register set contains 6 bytes) will be used to compare incoming destination addresses. Bit 8 corresponds to station address register set 0, bit 9 to register set 1, ... bit 13 to register set 5. A '1' in any bit enables that Station Address register set for reception. These bits are both read and write.

Bits 14-15: These two bits define the match modes for the Receiver logic.

15	14	Matchmode Description
0	0	Specific addresses only
0	1	Specific + broadcast addresses
1	0	Above + multicast addresses
1	1	All frames (promiscuous mode)

Configuration Register 2, A0-A3=010X

Bit 0: ByteSwap. The normal order for packing packet bytes into a 16 bit word is low byte first, i.e., the first byte of a packet is contained in bits 0 through 7, the second byte in bits 8 through 15. Setting this bit to a 1 causes the high and low order bytes to be swapped for data reads and writes to the Buffer Window Register when the 8005 is in 16 bit mode. Control registers are not affected. This bit has no effect when the 8005 is in 8 bit mode. It should not be changed when a DMA is in progress. Changing this bit will not affect the sequence of receive data bytes in the local buffer memory since the swap occurs on the system (Bus Interface) side of the buffer memory. This bit is both read and write.

Bit 1: Not Used. This bit should be written to '0' for future compatibility.

Bit 2: Not Used. This bit should be written to '0' for future compatibility.

Bit 3: CRC Error Enable. When set, the receiver will accept packets with CRC errors, place them in the local buffer and indicate that a packet is available via the Rx Interrupt Status bit.

Bit 4: Dribble Error. When set, the receiver will accept packets with a byte alignment error.

Bit 5: Short Frame Enable. When set, packets of less than 512 bits (64 bytes) exclusive of preamble and start packet delimiter bits, will be received and placed in the local buffer. Packets shorter than 6 bytes (2 bytes if bit 8 = 1) will always be rejected unless the Receiver is in promiscuous mode (all addresses match) or multicast/broadcast mode and the packet is a multicast/broadcast packet.

Bit 6: SlotSelect. This bit selects the slot time used to calculate backoff time following a collision. When a 0, which is the state after reset, the slot time is 512 bits and meets the IEEE 802.3 standard; when a 1, the slot time is 128 bits, the interframe spacing is 24 bits and the collision jam is 2 bytes long, which is useful for smaller networks such as serial backplane buses.

Bit 7: PreamSelect. When this bit is a 0, which is the state after reset, the 8005 automatically transmits an IEEE 802.3 compatible 64 bit preamble; when set to 1, the user must supply the preamble as part of the packet data. the preamble must still follow the 802.3 form in order to be recognized by other 8005's, but may have arbitrary length. Note that a minimum of 16 preamble bits are required by the 8005 on reception.

Bit 8: AddrLength. This bit selects the length of address to be used in address matching. When a 0, which is the state after reset, the length is 6 bytes, which conforms with the IEEE 802.3 standard; when set to 1 the length is 2 bytes, which is useful in limited networks such as serial backplane buses.

Bit 9: RecCrc. If set to a 1, received packets will include the CRC . If set to a 0, which is the state after reset, the 4 byte CRC will be stripped when received.

Bit 10: XmitNoCrc. If set to a 1, the Transmitter will not append the 4 byte frame check sequence to each packet transmitted. This is useful in local loopback to perform diagnostic checks, since it allows the software to provide its own CRC as the last four bytes of a packet to check the Receiver CRC logic. It is initialized to 0 after hardware or software reset.

Bit 11: Loopback. This bit controls the External Loopback pin. When set to a 1, the loopback output pin is at Vol; after reset or when cleared to a 0, the External Loopback output pin is at Voh.

Bit 12: CTRLO This bit controls the Control Output pin. When set to a 1, the CTRLO pin is at Voh; when cleared to 0 or after reset, this pin is at Vol.

Bits 13-14: Not used. Reserved for future use.

Bit 15: Reset. Writing a 1 to this bit is the same as asserting the hardware reset input. Reset should be followed by a 4 μs wait before attempting another access. Reads as a 0.

Receive End Area Register, A3-0 = 0110

Bits 0-7: ReaPtr. The Receive End Area pointer contains the high order byte of the local buffer address at which the Receive logic must stop to prevent writing over previously received packets. If the Receive logic reaches this address it will stop; the Receiver will be turned off and an interrupt will be issued. The Receiver can be re-started by freeing up buffer space and turning the Receiver back 'ON' again. It is both read and write.

Buffer Window Register, A3-0 = 100X

This register provides access to the area specified by the Buffer Code bits (bits 0-3) in Configuration Register #1. When the Buffer Code points to either the buffer memory (Buffer Code =1000₂), or the address PROM (Buffer Code = 0110₂), the address of the data transferred through this register is determined by the DMA pointer. All Buffer Code registers are byte wide except data.

Receive Pointer Register, A3-0 = 101X

The Receive pointer provides a 16 bit address that points to the next buffer memory location into which data or header information will be placed by the Receive logic. The low order 8 bits contain the least significant byte of the address. Prior to enabling the Receiver, this register should be set to point to the beginning of the Receive Area in the local buffer. This initial value should be remembered by system software since it will be the address of the first byte of the header block of the first packet received. While receiving, the Receive pointer will be incremented for each byte stored into the local buffer. When the Receive pointer increments past hex FFFF the most significant byte will be set equal to the value of the Transmit End Area + 1 and the least significant byte will be set to 00. Reading this register may be done at any time. It should be written only when the receiver is idle.

Transmit Pointer Register, A3-0 = 110X

The Transmit pointer points to the current location being accessed by the Transmit logic. Before starting the Transmitter, software loads this register with the address of the beginning of a transmit packet chain.

DMA Address Register, A3-0 = 111X

The DMA address register provides 16 bits of address information to the local buffer memory and 8 bits of address to the address PROM, depending on the buffer code written into Configuration Register 1. Its normal use is to provide an auto-incremented address to the local buffer so that the packet data can be moved via the Bus Interface. **When the DMA Address register is loaded, the DMA FIFO is cleared.** Therefore it is important to insure that the DMA FIFO is empty if it is in the write direction before loading the DMA register. When writing a packet to be transmitted, the DMA Address register automatically wraps around to 0000 when the Transmit End Area (contained in an indirect register, Buffer Code 0111) has been reached. When reading receive packets, the DMA Address register automatically wraps around to the Receive Start Area (Transmit End Area + 1,00) when address hex FFFF has been read.

Indirectly Accessed Registers

Infrequently used registers, such as, those normally loaded only when initially configuring the 8005, are accessed indirectly by first loading the Buffer Code bits in Configuration Register #1 with a code that points to the desired register. Reads and writes occur through the Buffer Window register. All indirect registers (a total of 38) are 8 bits wide, thus only D0-D7 are used.

Station Address Registers

The 8005 contains six 48-bit Station Address registers, which permits one network connection to provide up to 6 different server functions. Each of these Station Address registers is comprised of six 8-bit registers which must be loaded through the Buffer Window Register. Only those Station Address registers to be enabled for address matching need to be loaded.

To load a Station Address register, first turn the Receiver off. Select the desired station number (0-5) by writing the Buffer Code bits in Configuration Register #1. Next do 6 sequential **byte** writes to the Buffer Window register as follows: Write the least significant byte of the 6 byte Station Address; its low order bit, bit 0, will be the first bit received. Next write the remaining 5 bytes in ascending order. To read a Station Address register, first turn the receiver off by setting 'bit 12' Rx off on the Command register and verifying that the Receiver is off. Then select the desired station number by writing the Buffer Code bits in Configuration Register #1. Do 6 sequential reads to the Buffer Window Register; the first byte read will be the least significant byte. If the 8005 is configured to match 2 byte instead of 6 byte addresses, only the first 2 station address bytes are significant, although all 6 will read and write properly.

Transmit End Area Pointer

The 8-bit value of this pointer defines, with 256 location granularity, the end of the Transmit Packet Buffer area by specifying the highest value permitted in the most significant byte of the Transmit Pointer Register and, when loading a packet to be transmitted, the DMA Address register. It also indirectly defines the Receive Start Area address, since the Buffer Controller automatically calculates the high order byte of the address by adding 1 to the Transmit End Area pointer. To read or write this value, set Buffer Code = 0111, and do a read or write to the Buffer Window Register.

Interrupt Vector Register

This Read/Write register is accessed through the Buffer Window register when the Buffer Code in Configuration Register #1 is 9. It contains an 8 bit vector which is placed on data bits D0-D7 during an Interrupt Acknowledge cycle. If BUSMODE = 0, an Interrupt Acknowledge cycle is defined by INT* = 0, IACK* = 0, and READ/WRITE = 1. When BUSMODE = 1, an Interrupt Acknowledge cycle is defined by INT = 1, IACK* = 0, and IOR* = 0.

Other Buffer Window Register Uses

Address PROM Access

The 8005 supports access to up to 256 bytes of configuration data contained in a PROM or EEPROM. This can be used for any purpose, such as storing station addresses, register configurations, network connection data, etc. The address to the PROM is supplied by the DMA register through data bus bits D8-D15; the data lines from the PROM are connected to D0-D7. Chip select for the PROM is provided by output APEN*. Before accessing this PROM, insure that Transmit, Receive and DMA sections of the 8005 are disabled. Next load the PROM starting address which you wish to access into both the low byte and the high byte of DMA register. Set the Buffer Code bits in Configuration Register #1 to point to the address PROM. Each access to the Buffer Window register will chip enable the PROM, permitting reads. Successive accesses will increment the DMA register to point to the next byte in the PROM. If a 16 bit wide bus is used, the address supplied to the PROM will also be read on D8-D15.

Buffer Memory Access

The normal state of the Buffer Code bits, once the 8005 has been initialized with station addresses and buffer areas have been allocated, is with Buffer Memory selected. Access to the local buffer memory is provided by the DMA register, which automatically increments after each byte or word transfer. To write to the local buffer, set

Example of Chained Receive Frames

Bit #	7	6	5	4	3	2	1	0	
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	0	0	0	0	0	0	0	0	Next receive packet header goes here.
Addr. ptr2	0	0	0	0	0	0	0	0	
Header status	0	0	0	0	0	0	0	0	Last header in chain.
Packet status	0	0	0	0	0	0	0	0	

Packet Header Bytes

Transmit Header Command Byte (Byte #3)

7	6	5	4	3	2	1	0
1	Chain Con-tinue	Data Fol-lows	Not Used	Xmit Success Enable	16 Coll. Enable	Coll. Int. Enable	Babble Int. Enable

Receive Header Status Byte (Byte #3)

7	6	5	4	3	2	1	0
0	Chain Con-tinue	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

Transmit Packet Status Byte (Byte #4)

7	6	5	4	3	2	1	0
Done	← Reserved →				16 Coll.	Colli-sion	Bab-ble

Receive Packet Status Byte (Byte #4)

7	6	5	4	3	2	1	0
Done	Not Used	Not Used	Not Used	Short Frame	Drib. Error	CRC Error	Over-size

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8005 Configuration and Pointer Registers

Command (write only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Write	FIFO Read	Set Tx Off	Set Rx Off	Set DMA Off	Set Tx On	Set Rx On	Set DMA On	Buffer Window Ack	Tx Int Ack	Rx Int Ack	DMA Int Ack	Buffer Window Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Status (read only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Dir	FIFO Empty	FIFO Full	Not Used	Not Used	Tx On	Rx On	DMA On	Buffer Window Int	Tx Int	Rx Int	DMA Int	Buffer Window Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Configuration Register #1 (A3-0 = 001X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addr Match Mode	Addr Match Mode	Sta. 5 Enable	Sta. 4 Enable	Sta. 3 Enable	Sta. 2 Enable	Sta. 1 Enable	Sta. 0 Enable	DMA Burst Lngth	DMA Burst Lngth	DMA Burst Intvl	DMA Burst Intvl	Buffer Code 3	Buffer Code 2	Buffer Code 1	Buffer Code 0

Configuration Rgister #2 (A3-0 = 010X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	Not Used	Not Used	Control Output	Loop-Back	Xmit No CRC	Recv. CRC	Addr Leng.	Xmit No Pream	Slot Time Sel.	Short Frame Enable	Drib. Error Enable	CRC Error Enable	Not Used	Not Used	Byte Swap

Receive End Area Register (A3-0 = 0110 [2])

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	Receive End Area Pointer							

Receive Pointer Register (A3-0 = 101X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT RECEIVE BYTE															

Transmit Pointer Register (A3-0 = 110X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT TRANSMIT BYTE															

DMA Address Register (A3-0 = 111X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR SYTSEM READS OR WRITES															

Buffer Window Register (A3-0 = 100X [2])

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFFER CODE BITS DETERMINE SOURCE/DESTINATION FOR READS AND WRITES															

NOTES: 1. In 16 bit mode address A0 is a don't care for all registers except REA.
2. Both 8 and 16 bit modes.

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Station Address Register Format
2 of 6 Station Address Registers Shown

7	6	5	4	3	2	1	0

LEAST SIGNIFICANT BYTE
STATION ADDRESS REGISTER 0 BYTE 0
BUFFER CODE = 0000

STATION ADDRESS REGISTER 0 BYTE 1
BUFFER CODE = 0000

STATION ADDRESS REGISTER 0 BYTE 2
BUFFER CODE = 0000

STATION ADDRESS REGISTER 0 BYTE 3
BUFFER CODE = 0000

STATION ADDRESS REGISTER 0 BYTE 4
BUFFER CODE = 0000

STATION ADDRESS REGISTER 0 BYTE 5
BUFFER CODE = 0000
MOST SIGNIFICANT BYTE

7	6	5	4	3	2	1	0

LEAST SIGNIFICANT BYTE
STATION ADDRESS REGISTER 1 BYTE 0
BUFFER CODE = 0001

STATION ADDRESS REGISTER 1 BYTE 1
BUFFER CODE = 0001

STATION ADDRESS REGISTER 1 BYTE 2
BUFFER CODE = 0001

STATION ADDRESS REGISTER 1 BYTE 3
BUFFER CODE = 0001

STATION ADDRESS REGISTER 1 BYTE 4
BUFFER CODE = 0001

STATION ADDRESS REGISTER 1 BYTE 5
BUFFER CODE = 0001
MOST SIGNIFICANT BYTE

*the buffer code to select the buffer memory, set the FIFO direction to write (Command Register bits 14 and 15), load a starting address into the DMA register and write to the Buffer Window register. To read from the local buffer, the same steps as above must be followed except that the FIFO direction should be changed to the read direction **after** the DMA register has been written. This is the simplest way to access the local buffer as it requires no system DMA activity. It also permits network layer software to read network control data at the beginning of a received packet to determine if it is necessary to move the packet into global memory for further processing or simply reuse the area occupied by the packet by updating the Receive End Area register. For fastest transfer speed, e.g., to move packet data, an external system DMA Controller is supported via the DMA Request output, DMA Acknowledge input and Terminal Count input signals.*

Asynchronous Bus Control

The 8005 supports asynchronous bus control via the READY/DTACK* pin. By using READY/DTACK*, the cycle time minimums listed in the tables A thru' J need not be observed. READY/DTACK* takes care of these cycle times. This greatly simplifies the task of interfacing to the 8005 and also results in a higher overall data rate. To acheive the highest possible data rate, all data transfers should terminate within 100 ns of READY/DTACK* being asserted. This permits a sustained system bus transfer rate of 3.33 Mbytes/sec in 16 bit mode or 2.5 Mbytes/sec in 8 bit mode.

Absolute Maximum Stress Ratings

Temperature:

Storage .... −65°C to +150°C

Under Bias .... −10°C to +80°C

All Inputs and Outputs with

Respect to V_{SS} .... +6 V to −0.3 V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

V_{CC} Supply Voltage	5V ± 5%
Ambient Temperature	0°C to 70°C

DC Operating Charateristics (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I_{IL}	Input/Output Leakage		10	μA	$V_{IN} = V_{CC}$
			−10	μA	$V_{IN} = 0.1$ V
I_{CC}	Active I_{CC} Current @ $T_A = 0°C$		370	mA	CS* = V_{IL}, Outputs Open $T_A = 0°C$
	Active I_{CC} Current @ $T_A = 70°C$		280	mA	CS* = V_{IL}, Outputs Open $T_A = 70°C$
V_{IL1}	Input Low Voltage (except TXC*, RXC, CLK)	−0.3	0.8	V	
V_{IL2}	Input Low Voltage (TXC*, RXC, CLK)	−0.3	0.4	V	
V_{IH1}	Input High Voltage (except TXC*, RXC, CLK)	2.0	$V_{CC} + 1$	V	
V_{IH2}	Input High Voltage (TXC*, RXC, CLK)	3.5	$V_{CC} + 1$	V	
V_{OL1}	Output Low Voltage (except AD_{0-7})		0.40	V	$I_{OL} = 2.1mA$
V_{OL2}	Output Low Voltage (AD_{0-7})		0.40	V	$I_{OL} = 200$ μA
V_{OH1}	Output High Voltage (except AD_{0-7})	2.4		V	$I_{OH} = −400$ μA
V_{OH2}	Output High Voltage (AD_{0-7})	2.4		V	$I_{OH} = −200$ μA

A.C. Test Conditions

Output Load:
  AD0-AD7, I(load) = ± 200 μA
  C(load) = 50 pF.
  All Other Outputs: 1 TTL Gate and C(load) = 100 pF.
Input Rise and Fall Times (except TXC, RXC, CLK):
  10 ns maximum.

Input Rise and Fall Times (TXC, RXC, CLK):
  5 ns maximum.
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
  Inputs: 1 V and 2 V
  Outputs: 0.8 V and 2 V

Capacitance [1]   Ambient Temperature = 25°C, F = 1 MHz

| Symbol | Parameter | Limits | | Unit | Test Condtion |
		Min.	Max.		
C_{IN}	Input Capacitance		15	pF	$V_{IN} = 0$
C_{OUT}	Output Capacitance		15	pF	$V_{OUT} = 0$

Electrostatic Discharge Characteristics

Symbol	Parameter	Value	Test Condtion
V_{ZAP}[2]	E.S.D. Tolerance	> 2000 V	Mil-STD 883 Meth. 3015

NOTES: 1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table A. Bus Write Cycle — BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	15		ns
2	TRWLCSL	R/W* Setup Time	0		ns
3	TCSLCSH	CS* Pulse Width	100		ns
4	TDVCSH	Data Setup Time	70		ns
5	TCSHDX	Data Hold Time	20		ns
6	TCSLDTL	DTACK* Assertion Delay[4]		60	ns
7	TCSHDTH	DTACK* Deassertion Delay		60	ns
8	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
9	TCSHAX	Address Hold Time	20		ns
10	TCSHRWX	R/W* Hold Time	20		ns
11	TCSHCSL	CS* High Time[5] a. FIFO Data Write[6] b. Configuration Regs[2] c. Pointer Regs.	 200 350 350		ns ns ns
12	TCSHDTL	Write Recovery Time: a. FIFO Data Write[1] b. Configuration Regs [1,2] c. Pointer Regs. [3]		 800 800 1800	ns ns ns ns
13	TCSLENL	EN* Assert Delay		50	ns
14	TCSHENH	EN* Deassert Delay		50	ns
15	TCSLDTV	CS* Assert to DTACK* Valid		50	ns

NOTES:

1. Write Recovery Time is for 16 bit writes. If BUSSIZE = 0 (8 bit writes), subtract 200 ns.
2. Configuration Registers are: Command/Status Register, Configuration Register #1 & 2, Interrupt Vector Register, and Station Address Registers.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA register. If BUSSIZE = 0, subtract 600 ns.
4. The trailing edge of CS* initiates an internal write sequence. Should another CS* occur during this time, the assertion of DTACK* will be delayed until the internal write sequence has finished (Ref. # 12, TCSHDTL).
5. After changing the Buffer Code (Config. Reg. #1 bits 0-3), Ref. #11 must be increased to 800 ns before a Buffer Window access is done in order to allow time for the new Buffer Code to propagate internally.
6. The 200 ns minimum time applies for writes to packet buffer. If the preceding write operation was to a configuration register or pointer register, the CS* high time is 350 ns minimum for first write to the packet buffer. Subsequent writes to the packet buffer can occur with 200 ns min. CS* high time.
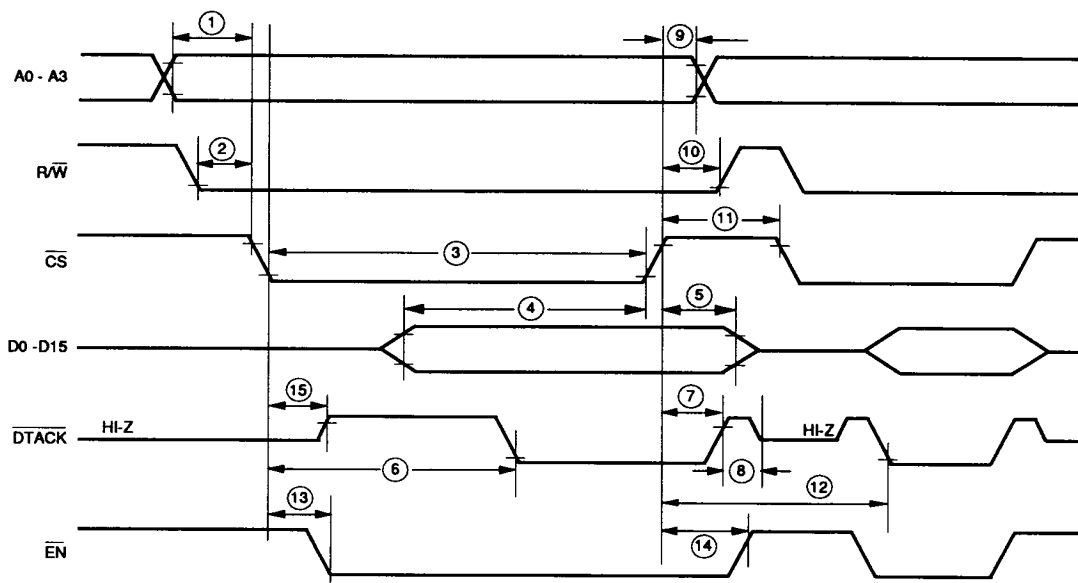
Figure A. Bus Write Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table B. Bus Read Cycle — BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	15		ns
2	TRWHCSL	R/W* Setup Time	0		ns
3	TCSLDTL	DTACK* Assert Delay a. FIFO Data[1] b. Configuration Regs.[2] c. Other Pointer Regs.[3]		 60 800 1800	ns ns ns ns
4	TDTLDV	Time from DTACK* Asserted to Data Valid		50	ns
5	TCSLCSH	CS* Pulse Width	100		ns
6	TCSHDTH	DTACK* Deassertion Delay		60	ns
7	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
8	TCSHDZ	Data Hi-Z Delay		100	ns
9	TCSHDX	Data Hold Time	20		ns
10	TCSHRWX	R/W* Hold Time	20		ns
11	TCSHAX	Address Hold Time	20		ns
12	TCSHCSL	CS* High Time	200		ns
13	TCSLAPL	APEN* Assert Delay		400	ns
14	TCSHAPH	APEN* Deassert Delay		50	ns
15	TCSLENL	EN* Assert Delay		50	ns
16	TCSHENH	EN* Deassert Delay		50	ns
17	TCSLDTV	CS* Assert to DTACK* Valid		50	ns

NOTES:

1. The BIU prefetches one word (byte) of FIFO data. Thus, data is generally available immediately and DTACK* will assert within 50 ns. Following the read, the BIU will fetch the next word (byte) of data. Should another data read occur before the BIU has completed the prefetch, DTACK* will be delayed until the prefetch is completed. The assert delay in this case is 650 ns max (450 ns in 8 bit mode).
2. Configuration Registers are: Command/Status Register, Configuration Register # 1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers. If BUSSIZE = 0 (8 bit reads), subtract 200 ns.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register. If BUSSIZE = 0, subtract 600 ns.
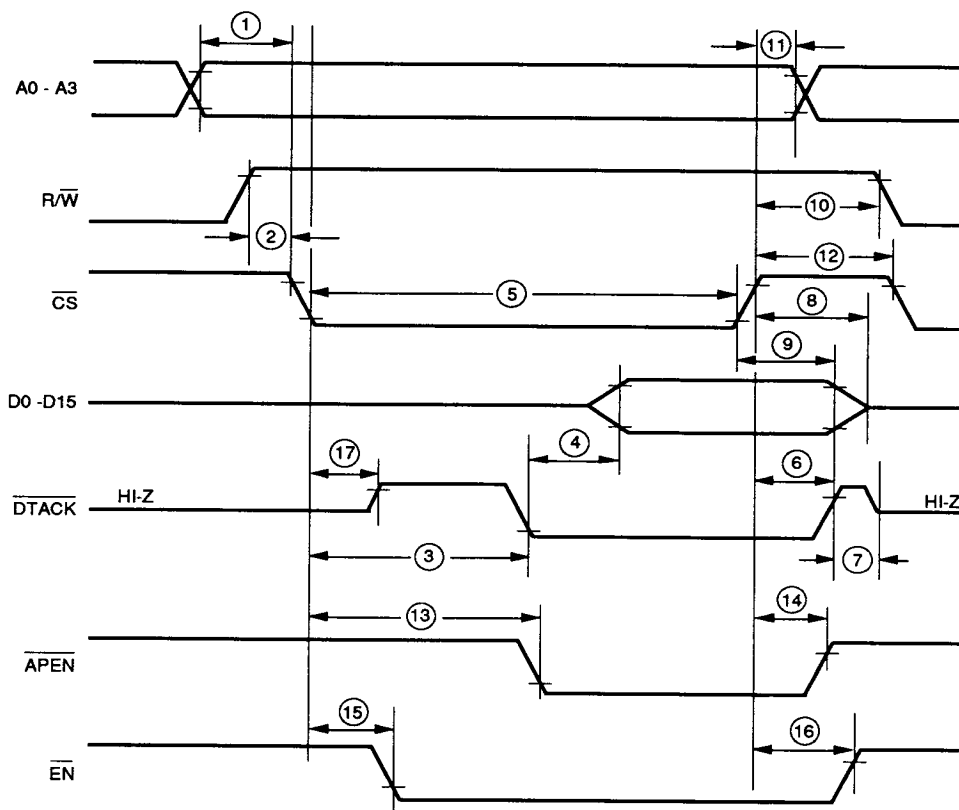
Figure B. Bus Read Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table C. Interrupt Cycle — BUSMODE = 0

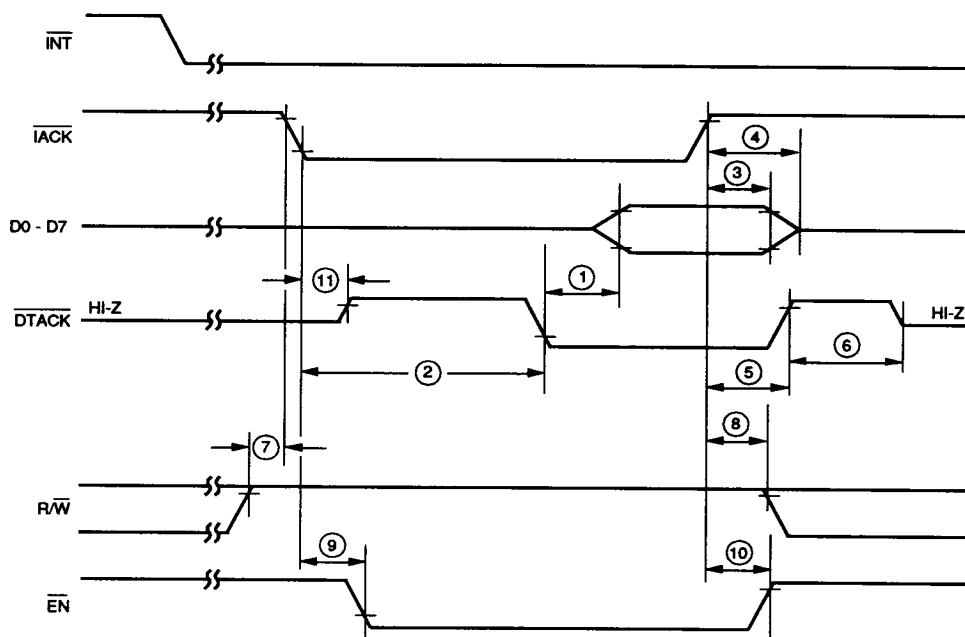| Ref. #	Symbol	Description	Min.	Max.	Units
1	TDTLDV	Time from DTACK* Assert to Data Valid		50	ns
2	TIALDTV	DTACK* Assert Delay		600	ns
3	TIAHDX	Data Hold from IACK* Deassert	20		ns
4	TIAHDZ	Data Hi-Z from IACK* Deassert		100	ns
5	TIAHDTH	DTACK* Deassert Delay		60	ns
6	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
7	TRWHIAL	R/W* Setup Time	15		ns
8	TIAHRWX	R/W* Hold Time from IACK*	20		ns
9	TIALENL	EN* Assert Delay		50	ns
10	TIAHENH	EN* Deassert Delay		50	ns
11	TIALDTV	IACK* Assert to DTACK* Valid		50	ns

Figure C. Interrupt Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table D. DMA Read Cycle — BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRWHDAL	R/W* Setup Time	30		ns
2	TDALDAH	DACK* Pulse Width[1]	100		ns
3	TDTLDV	Time from DTACK* Asserted to Data Valid		50	ns
4	TDAHDX	Data Hold Time	20		ns
5	TDAHDZ	Data Hi-Z Delay		100	ns
6	TDAHDAL	DACK* High Time	200		ns
7	TDAHRWX	R/W* Hold Time	20		ns
8	TDALTCL	TERMCT* Asserted While DACK* Asserted	125		ns
9	TTCLDRH	DREQ* Delay[5]		175	ns
10	TDALDRH	DREQ Delay After End of DMA Burst[6]		100	ns
11	TDALDTL1	DTACK* Assertion Delay[2]		60	ns
12	TDAHDTH	DTACK* Deassertion Delay		60	ns
13	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
14	TDALENL	EN* Assert Delay		50	ns
15	TDAHENH	EN* Deassert Delay		50	ns
16	TDALDTV	DACK* Assert to DTACK* Valid		50	ns
17	TDALDTL2	Read Recovery Time[3,4]		800	ns

NOTE:
1. DACK* must be asserted until DTACK* is asserted and for a minimum of 100 ns.
2. This delay applies only if the 8005 is "ready" when DACK* is asserted i.e. the first read of a burst, or a read that occurs after the Ref. #17 TDALDTL2 period has elapsed.
3. The BIU pre-fetches FIFO data. Thus, data is available immediately for the first read of any burst. Once the BIU detects a read operation, it begins fetching the next byte or word of data. This occurs during the Ref. #17 TDALDTL2 period. If a subsequent DACK* occurs within the Ref. #17 TDALDTL2 period, DTACK* will stay de-asserted until the FIFO data has been fetched. If the subsequent DACK* does not occur until after the Ref. #17 TDALDTL2 period has elapsed, then the 8005 is "ready" and Ref. #11 TDALDTL1 applies.
4. Subtract 200 ns if BUSSIZE = 0 (8 bit mode).
5. DACK* and TERMCT* must both be active at the same time and for a minimum of 125 ns. The de-assertion of DREQ* is timed from the last one to assert.
6. Ref. #10 TDALDRH applies for normal DMA burst terminations — not those due to TERMCT.

All the timing in this table also apply when reading data with programmed I/O; CS* replaces DACK* and the DREQ* and TERMCT* signals do not apply. A0-A3 setup times are the same as R/W*.
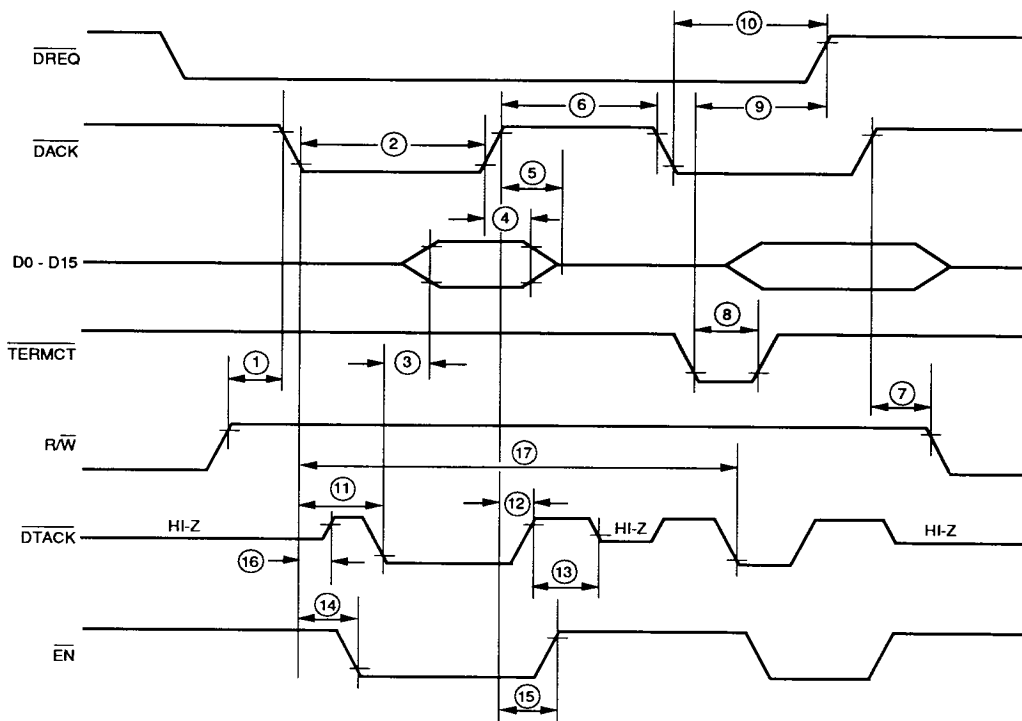
Figure D. DMA Read Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table E. DMA Write Cycle — BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRWLDAL	R/W* Setup Time	30		ns
2	TDALDAH	DACK* Pulse Width[1]	100		ns
3	TDVDAH	Data Setup Time	70		ns
4	TDAHDX	Data Hold Time	20		ns
5	TDAHDAL	DACK* High Time	200		ns
6	TDALTCL	TERMCT* Asserted While DACK* Asserted	125		ns
7	TDAHRWX	R/W* Hold Time	20		ns
8	TTCLDRH	DREQ* Delay[5]		175	ns
9	TDALDRH	DREQ Delay After End of DMA Burst[6]		100	ns
10	TDALDTL	DTACK* Assertion Delay[2]		60	ns
11	TDAHDTH	DTACK* Deassertion Delay		60	ns
12	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
13	TDALENL	EN* Assert Delay		50	ns
14	TDAHENH	EN* Deassert Delay		50	ns
15	TDALDTV	DACK* Assert to DTACK* Valid		50	ns
16	TDAHDTL	Write Recovery Time[3,4]		800	ns

NOTES:
1. DACK* must be asserted until DTACK* is asserted and for a minimum of 100 ns.
2. This delay applies only if the 8005 is "ready" when DACK* is asserted i.e. the first write of a burst, or a write that occurs after Ref. # 16 TDAHDTL period has elapsed.
3. The trailing edge of DACK* initiates an internal write sequence that lasts a maximum of 800 ns in 16 bit mode. Should another DACK* occur during this period, DTACK* will remain de-asserted until Ref. #16 TDAHDTL period has elapsed. If the subsequent DACK* does not occur until after the internal write sequence has ended, then the 8005 is "ready" and Ref. # 10 TDALDTL applies.
4. Subtract 200 ns when BUSSIZE = 0 (8 bit mode).
5. DACK* and TERMCT* must both be active at the same time and for a minimum of 125 ns. The de-assertion of DREQ* is timed from the last one to assert.
6. Ref. #9 TDALDRH applies for normal DMA burst terminations — not those due to TERMCT.

All the timing in this table also apply when writing data with programmed I/O; CS* replaces DACK* and the DREQ*, TERMCT* signals do not apply. A0-A3 times are the same as R/W*.
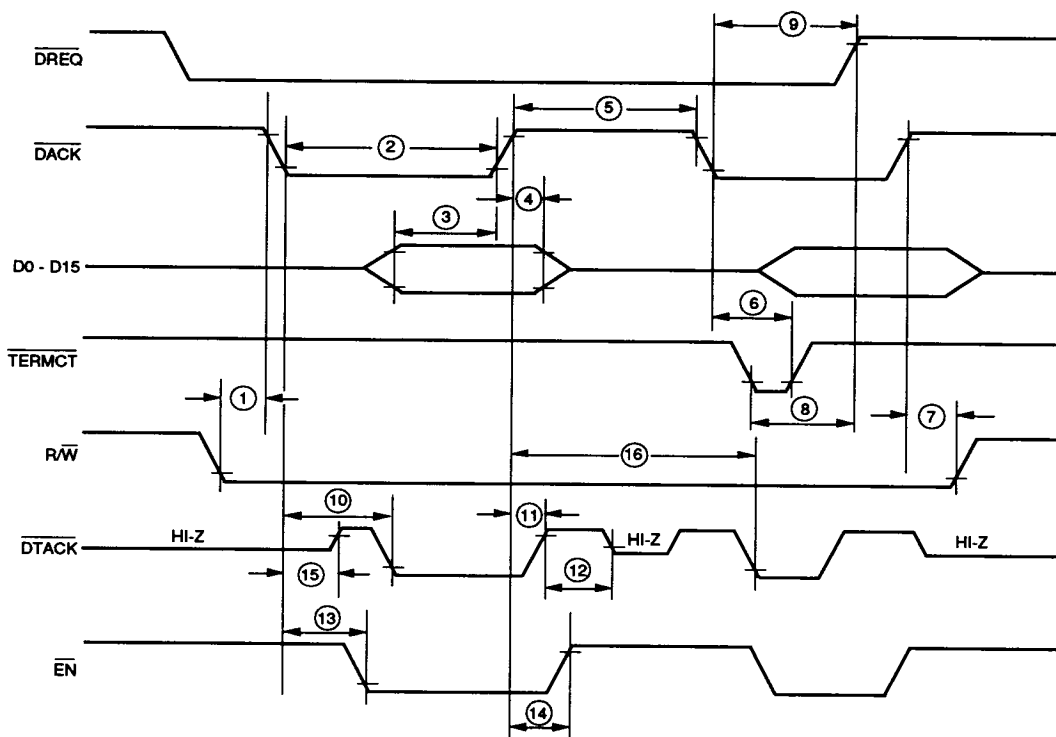
Figure E.   DMA Write Cycle Timing Diagram — BUSMODE = 0

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A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V$_{cc}$ range, unless otherwise specified)

Table F. Bus Write Cycle — BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVWL	Address Setup Time	30		ns
2	TCSLWL	CS* Setup Time	30		ns
3	TWLWH	IOW* Pulse Width	100		ns
4	TDVWH	Data Setup Time	70		ns
5	TWHDX	Data Hold Time	20		ns
6	TWLRYL	READY Deassert Delay		35	ns
7	TCSLRYV	CS* Asserted to READY Valid[4]		50	ns
8	TCSHRYZ	READY Delay to Hi-Z		50	ns
9	TWHAX	Address Hold Time	20		ns
10	TWHCSH	CS* Hold Time	20		ns
11	TWHWL	IOW* High Time[5] a. FIFO Data Write[6] b. Configuration Regs. [2] c. Pointer Registers	 200 350 350		 ns ns ns
12	TWHRYH	Write Recovery Time: a. FIFO Data Write[1] b. Configuration Regs. [1,2] c. Pointer Registers. [3]		 800 800 1800	ns ns ns ns
13	TCSLENL	EN* Assert Delay		50	ns
14	TCSHENH	EN* Deassert Delay		50	ns

NOTES:

1. Recovery time is for 16 bit writes. If BUSSIZE = 0 (8 bit writes), subtract 200 ns.
2. Configuration Registers are: Command/Status Register, Configuration Register #1, & 2, Interrupt Vector Register, and Station Address Registers.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA Register. If BUSSIZE = 0, subtract 600 ns.
4. The trailing edge of IOW* initiates an internal write sequence. Should another IOW* occur during this sequence, READY de-asserts (Ref. # 6 TWLRYL) and then asserts after the internal write sequence has finished (Ref. #12 TWHRYH). If the subsequent IOW* does not occur until after the internal write sequence has ended, then Ref. # 6 TWLRYL has no meaning since READY does not de-assert under this condition.
5. After changing the Buffer Code (Config. Reg. #1 bits 0-3), Ref. #11 must be increased to 800 ns before a Buffer Window access is done in order to allow time for the new Buffer ZCode to propagate internally.
6. The 200 ns minimum time applies for writes to packet buffer. If the preceding write operation was to a configuration register or pointer register, the CS* high time is 350 ns minimum for first write to the packet buffer. Subsequent writes to the packet buffer can occur with 200 ns min. CS* high time.
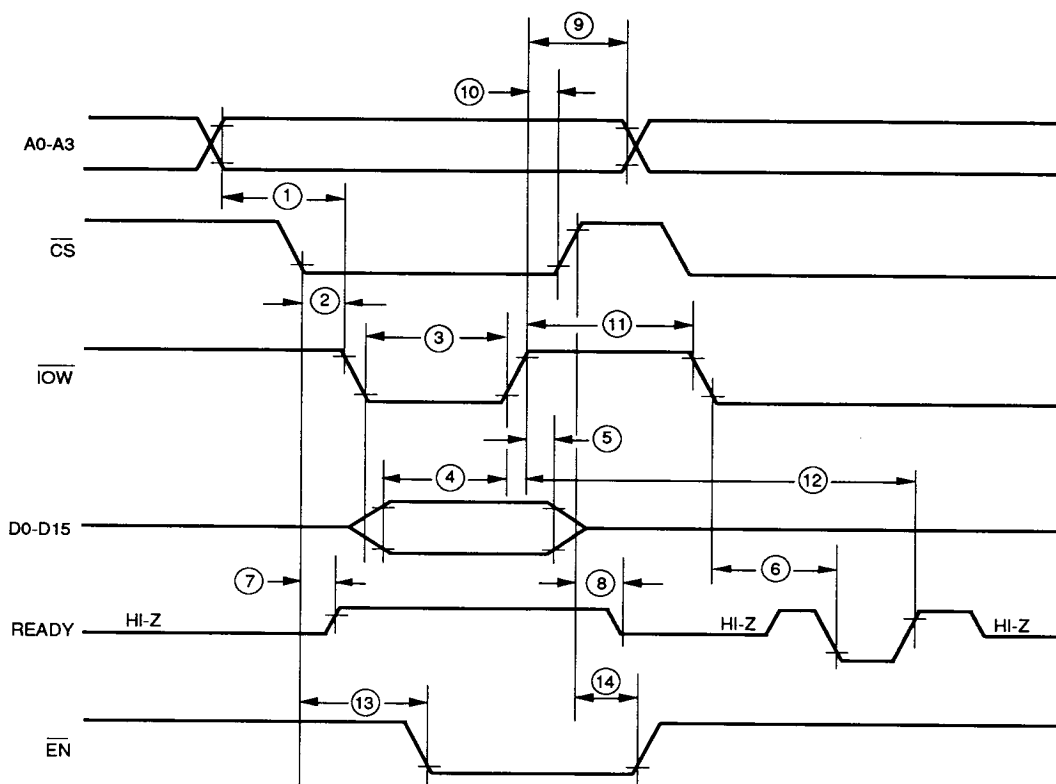
Figure F. Bus Write Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table G. Bus Read Cycle — BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRL	Address Setup Time	30		ns
1a	TCSLRL	CS* Setup Time	30		ns
2	TRHRL	IOR* High Time	200		ns
3	TRLRYH	READY Assert Delay a. FIFO Data [1] b. Configuration Regs.[2] c. Pointer Registers.[3]		 35 800 1800	ns ns ns ns
4	TRLRYL	READY Deassertion Delay		35	ns
5	TRYHDV	READY Assert to Data Valid		50	ns
6	TCSHRYZ	READY Delay to Hi-Z		50	ns
7	TRHDX	Data Hold Time	20		ns
8	TRHDZ	Data Delay to Hi-Z		100	ns
9	TRHAX	Address Hold Time	20		ns
10	TRHCSH	CS* Hold Time	20		ns
11	TRLRH	IOR* Pulse Width	100		ns
12	TRLAPL	APEN* Assert Delay		400	ns
13	TRHAPH	APEN* Deassert Delay		50	ns
14	TCSLENL	EN* Assert Delay		50	ns
15	TCSHENH	EN* Deassert Delay		50	ns
16	TCSLRYV	CS* Assert to READY Valid		50	ns

NOTES:

1. The BIU prefetches one word (byte) of FIFO data. Thus, data is generally available immediately and READY will not de-assert during a data read. Following the read, the BIU will fetch the next word (byte) of data. Should another data read occur before the BIU has completed the prefetch, READY will first de-assert and then assert after the prefetch is completed. The assert delay in this case is 800 ns max (600 ns in 8 bit mode).
2. Configuration Registers are: Command/Status Register, Configuration Register # 1, & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers. If BUSSIZE = 0 (8 bit reads), subtract 200 ns.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register. If BUSSIZE = 0, subtract 600 ns.
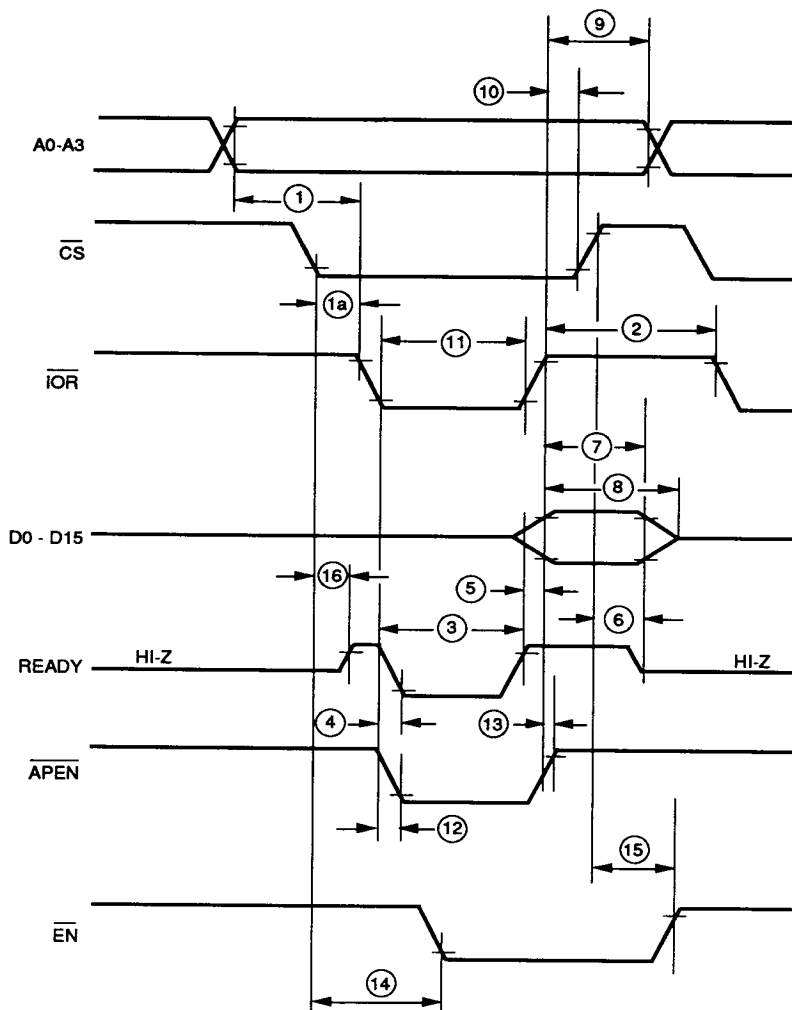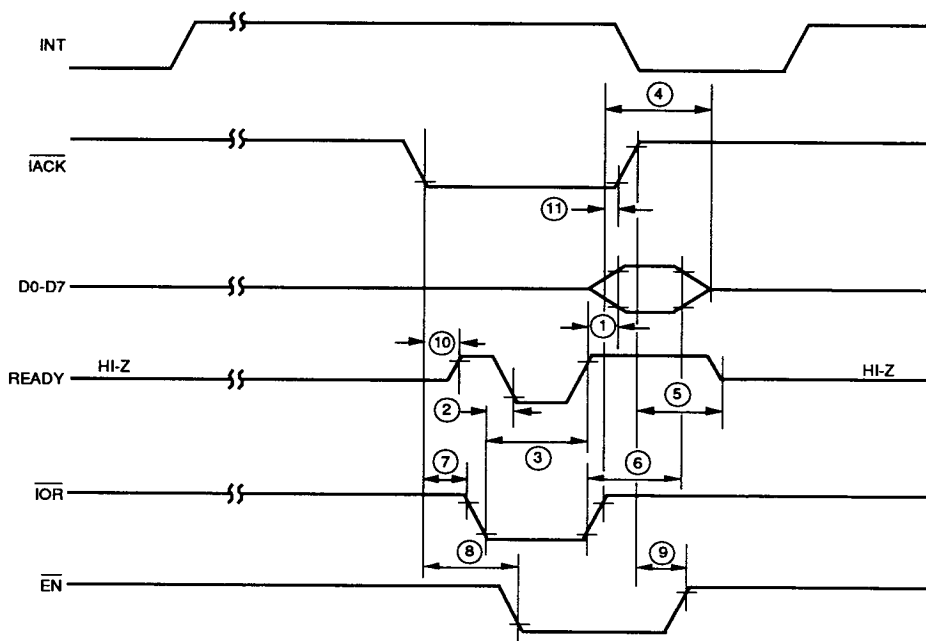
Figure G.   Bus Read Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table H. Interrupt Cycle — BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRYHDV	READY Assert to Data Valid		50	ns
2	TRLRYL	READY Deassertion Delay		35	ns
3	TRLRYH	READY Assert Delay		600	ns
4	TRHDZ	Data Delay to Hi-Z		100	ns
5	TIAHRYZ	READY Delay to Hi-Z		50	ns
6	TRHDX	Data Hold from IOR*	20		ns
7	TIALRL	IACK* Setup Time	30		ns
8	TIALENL	EN* Assert Delay		50	ns
9	TIAHENH	EN* Deassert Delay		50	ns
10	TIALRYV	IACK* Assert to READY Valid		50	ns
11	TRHIAH	IACK* Hold Time from IOR*	20		ns

Figure H. Interrupt Cycle Timing Diagram — BUSMODE = 1

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A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table I. DMA Write Cycle — BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TDALWL	DACK* Setup Time	30		ns
2	TWLWH	IOW* Pulse Width[1]	100		ns
3	TDVWH	Data Setup Time	70		ns
4	TWHDX	Data Hold Time	20		ns
5	TWHWL	IOW* High Time	200		ns
6	TTCHTCL	TERMCT Asserted While DACK* Asserted	125		ns
7	TTCHDRL	DREQ Delay from TERMCT[4]		175	ns
8	TWLDRL	DREQ Delay from IOW*[5]		100	ns
9	TWHDAH	DACK* Hold Time	20		ns
10	TDALENL	EN* Assert Delay		50	ns
11	TDAHENH	EN* Deassert Delay		50	ns
12	TWLRYL	READY Deassert Delay[2]		35	ns
13	TWHRYH	Write Recovery Time [3]		800	ns
14	TDAHRYZ	READY Delay to Hi-Z		50	ns
15	TDALRYV	DACK* Asserted to READY Valid		50	ns

NOTES:
1. IOW* must be asserted until READY is asserted and for a minimum of 100 ns.
2. The trailing edge of IOW* initiates an internal write sequence that lasts a maximum of 800 ns in 16 bit mode. Should another IOW* occur during this period, READY de-asserts (Ref. #12 TWLRYL) and then asserts after the internal write sequence has finished (Ref. #13 TWHRYH). If the subsequent IOW* does not occur until after the internal write sequence has ended, then Ref. #12 TWLRYL has no meaning since READY does not de-assert under this condition.
3. Subtract 200 ns when BUSSIZE = 0 (8 bit mode).
4. DACK* and TERMCT must both be asserted at the same time and for a minimum of 125 ns. The de-assertion of DREQ is timed from the last one to assert.
5. Ref. #8 TWLDRL applies for normal DMA burst terminations — not those due to TERMCT.

All the timing in this table also apply when writing data with programmed I/O; CS* replaces DACK* and the DREQ*, TERMCT signals do not apply. A0-A3 times are the same as CS*.
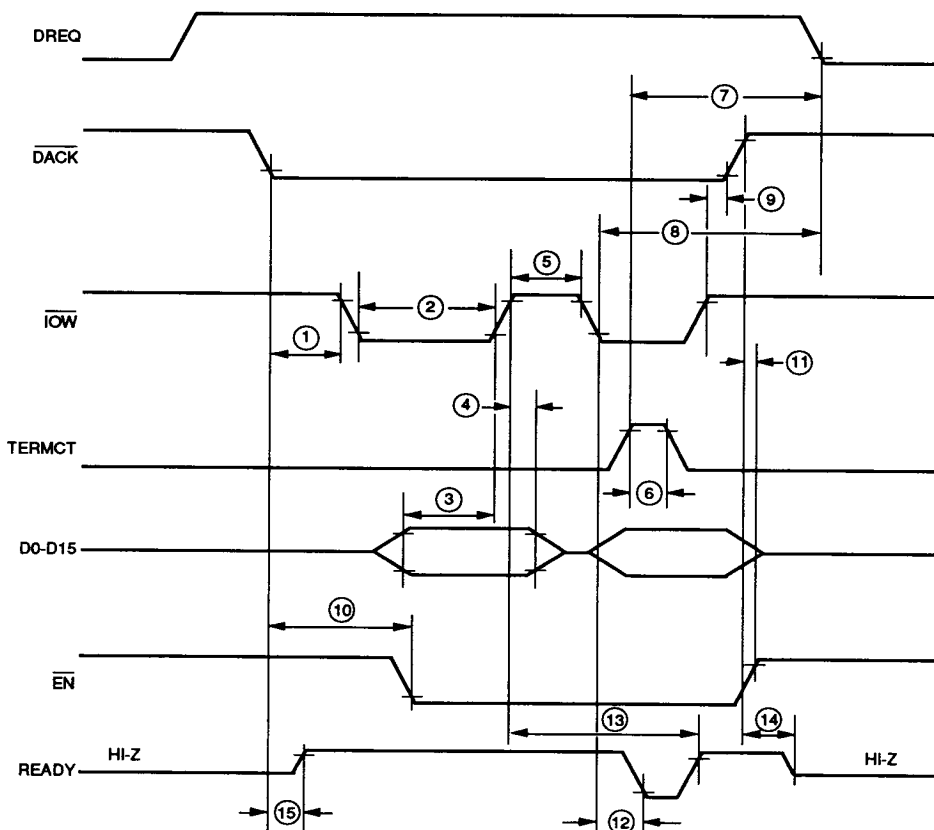
Figure I. DMA Write Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table J. DMA Read Cycle — BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TDALRL	DACK* Setup Time	30		ns
2	TRLRH	IOR* Pulse Width[1]	100		ns
3	TDVRYH	READY Asserted to Data Valid		50	ns
4	TRHDX	Data Hold Time	20		ns
5	TRHRL	IOR* High Time	200		ns
6	TTCHTCL	TERMCT Asserted While DACK* Asserted	125		ns
7	TTCHDRL	DREQ Delay from TERMCT[4]		175	ns
8	TRLDRL	DREQ Delay from IOR*[5]		100	ns
9	TRHDAH	DACK* Hold Time	20		ns
10	TRHDZ	Data Hi-Z Delay		100	ns
11	TDALENL	EN* Assert Delay		50	ns
12	TDAHENH	EN* Deassert Delay		50	ns
13	TRLRYL	READY Deassert Delay[2]		35	ns
14	TRLRYH	Read Recovery Time[3]		800	ns
15	TDAHRYZ	READY Delay to Hi-Z		50	ns
16	TDALRYV	DACK* Assert to READY Valid		50	ns

NOTES:
1. IOR* must be asserted until READY is asserted and for a minimum of 100 ns.
2. The BIU pre-fetches FIFO data. Thus, data is available immediately for the first read of any burst. Once the BIU detects a read operation, it begins fetching the next byte or word of data. This occurs during the Ref. #14 TRLRYH period. If a subsequent IOR* occurs within the Ref. #14 TRLRYH period, READY will de-assert (Ref. #13 TRLRYL) and then assert after the FIFO data has been fetched. If the subsequent IOR* does not begin until Ref. #14 has ended, then Ref. #13 has no meaning since READY does not de-assert under this condition.
3. Subtract 200 ns if BUSSIZE = 0 (8 bit mode).
4. DACK* and TERMCT must be asserted at the same time and for a minimum of 125 ns. The de-assertion of DREQ is timed from the last one to assert.
5. Ref. #8 TRLDRL applies for normal DMA burst terminations — not those due to TERMCT.

All the timing in this table also apply when reading data with programmed I/O: CS* replaces DACK* and the DREQ, TERMCT signals do not apply. A0-A3 times are the same as CS*.
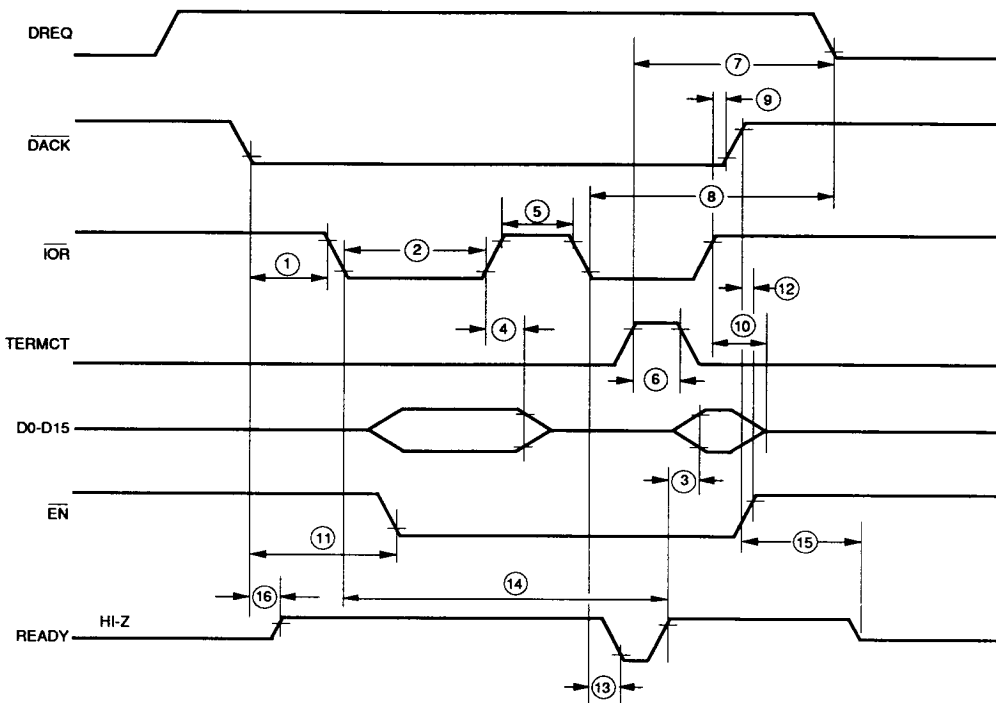
Figure J. DMA Read Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table K. Local Buffer Read or Write Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRSLAX	Row Address Hold Time	100		ns
2	TAVRSL	Row Address Setup Time	25		ns
3	TRSHRSL	RAS* Pulse Width High	200		ns
4	TCSLAX	Column Address Hold Time	45		ns
5	TAVCSL	Column Address Setup Time	10		ns
6	TCSHCSL	CAS* Pulse Width — High	60		ns
7	TCSLCSH	CAS* Pulse Width — Low	110		ns
8	TAZGL	Address Hi-Z to G* Low Time	0		ns
9	TGLCSH	G* Setup Time to CAS*	70		ns
10	TGLDV	G* to Data Valid		40	ns
11	TCSHDX	Data Hold from CAS Deassert	0		ns
12	TCSHDZ	Data Hi-Z from CAS Deassert		40	ns
13	TAVAV	Read or Write Cycle Time a. Single Cycle b. Page Mode	 600 200		 ns ns
14	TDVWL	Data Setup Time	5		ns
15	TWLDX	Data Hold Time	60		ns
16	TWLWH	Write Pulse Width	60		ns
17	TCSLWL	CAS* Setup to W*	60		ns
18	TWLCSH	Write Setup Time	40		ns
19	TRSLRSL	RAS* Cycle Time	600		ns

NOTE: TMS 4464-10, −12 or equivalent satisfies the above timing.

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
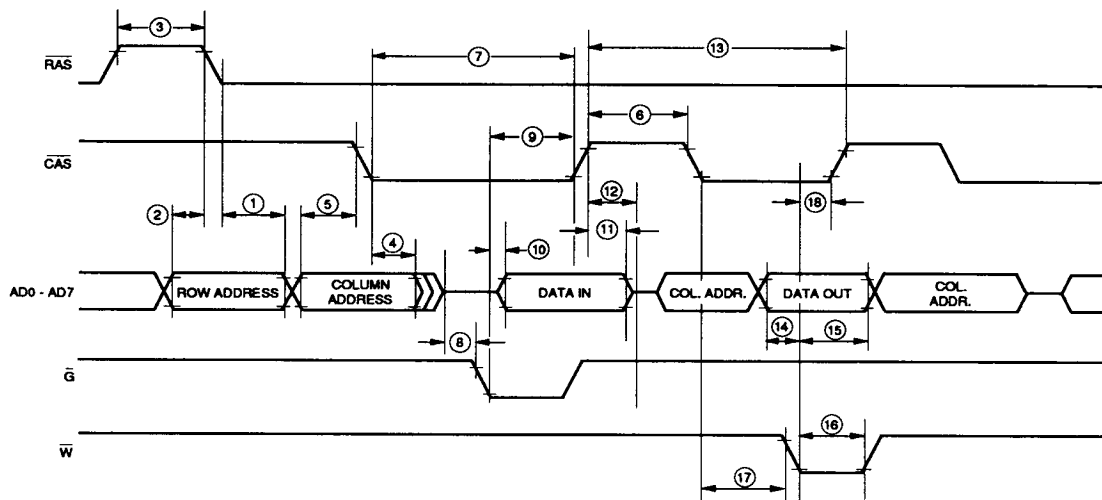(Over operating temperature and V_{cc} range, unless otherwise specified)

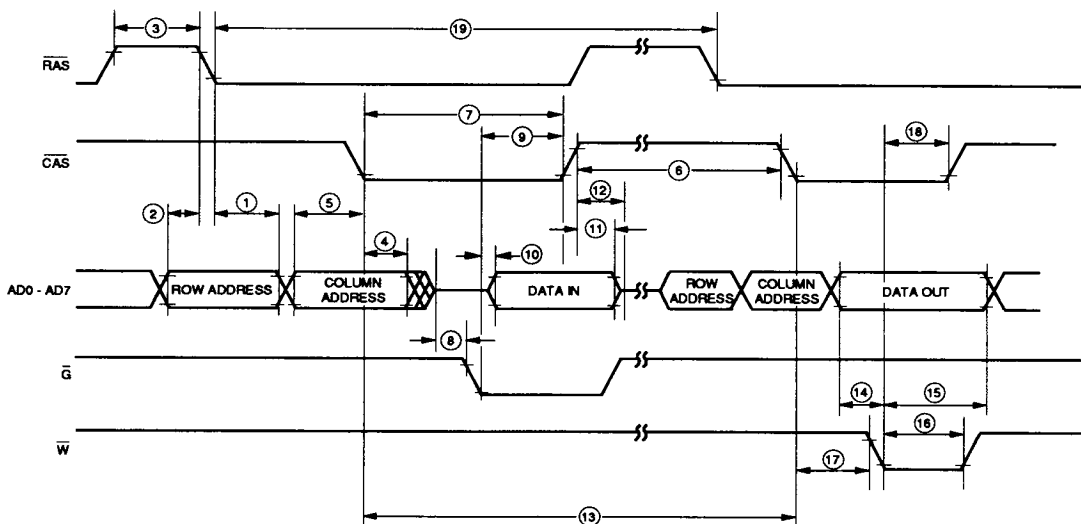**Figure K1. Local Dram Buffer Page-Mode Read and Write Cycle Timing Diagram**

Figure K2. Local Dram Buffer Single Cycle Read and Write Cycle Timing Diagram

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table L. Local Buffer Refresh Cycle

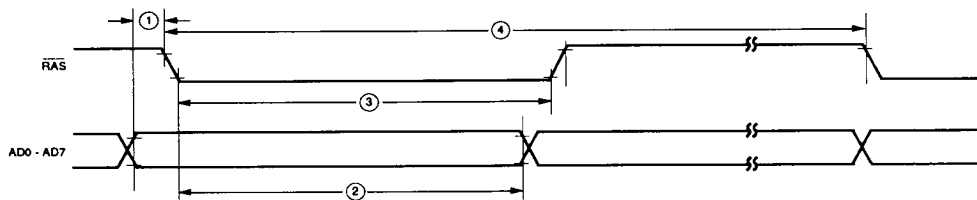| Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRSL	Address Setup Time to RAS*	25		ns
2	TRSLAX	Address Hold Time from RAS*	100		ns
3	TRSLRSH	RAS* Pulse Width	200		ns
4	TRSLRSL	RAS* Cycle Time	400		ns

Figure L. Local Dram Buffer Refresh Cycle Timing Diagram

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table M. Serial Interface Timing

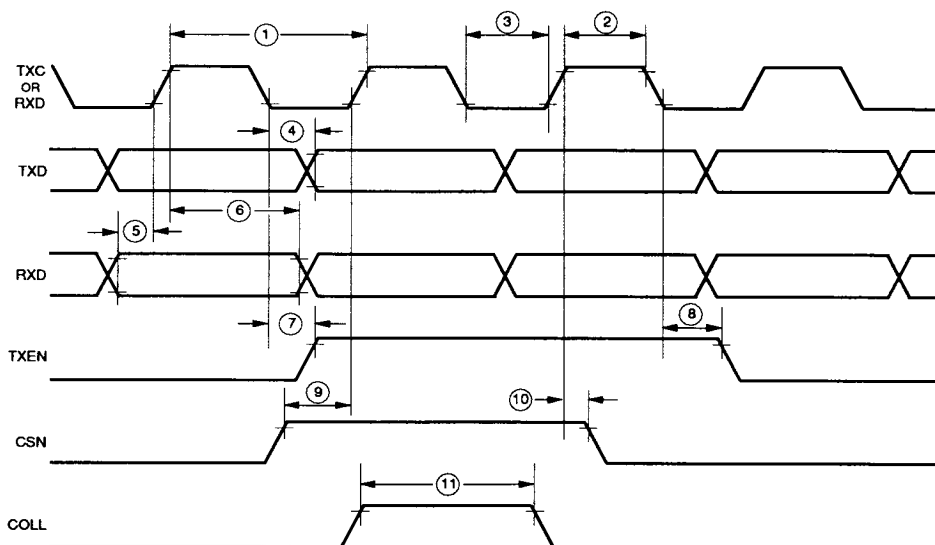| Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKH	TXC*/RXC Cycle Time	100		ns
2	TCKHCKL	TXC*/RXC High Width	45		ns
3	TCKLCKH	TXC*/RXC Low Width	45		ns
4	TCKLDV	TXD Delay from TXC*		60	ns
5	TDVCKH	RXD Setup to RXC	30		ns
6	TCKHDX	RXD Hold Time from RXC	20		ns
7	TCKLTEH	TXEN Delay from TXC*		60	ns
8	TCKLTEL	TXEN Hold Time from TXC*	20		ns
9	TCSHCKH	CSN Setup to RXC	20		ns
10	TCKHCSL	CSN Hold Time from RXC	20		ns
11	TCHCL	COLL Pulse Width	200		ns

Figure M. Serial Transmit & Receive Interface Timing

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{cc} range, unless otherwise specified)

Table N. Master Clock and Reset Timing

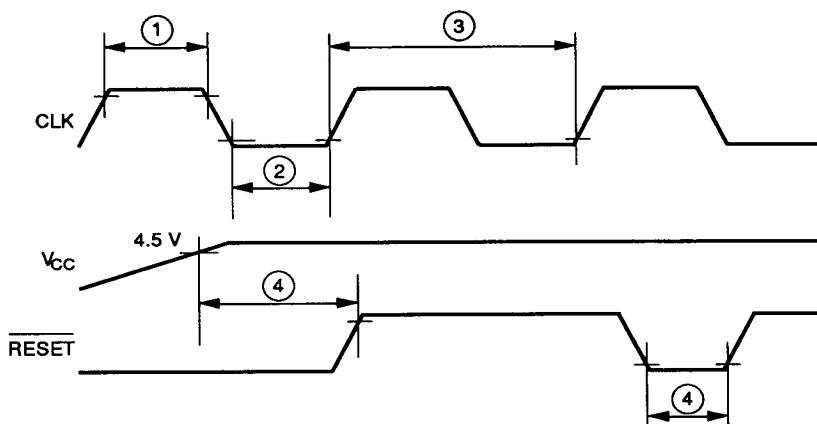| Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKL	CLK Pulse Width High	15	25	ns
2	TCKLCKH	CLK Pulse Width Low	15	25	ns
3	TCKHCKH	CLK Cycle Time	49.9	50.1	ns
4	TRSLRSH	Reset Pulse Width	1		μs

Figure N. Master Clock and Reset Timing

Ordering Information

PART NUMBER

N   Q   8005

PRODUCT: 8005 ADVANCED EDLC

TEMPERATURE RANGE: Q = 0° TO 70°C

PACKAGE TYPE: N = 68 PIN PLCC

seeq *Technology, Incorporated*