MEMC Datasheet

Part No 0460,019
Issue No 1.0
30 September 1986

ISBN 1 85250 025 5

Published by:
Acorn Computers Limited, Fulbourn Road, Cherry Hinton, Cambridge CB1 4JN, UK

Contents

1. Introduction

The Memory Controller (MEMC) acts as the interface between the ARM (Acorn RISC Machine) processor, Video Controller (VIDC), I/O Controllers (including IOC), Read-Only memories (ROM) and Dynamic memory devices (DRAM), providing all the critical system timing signals.

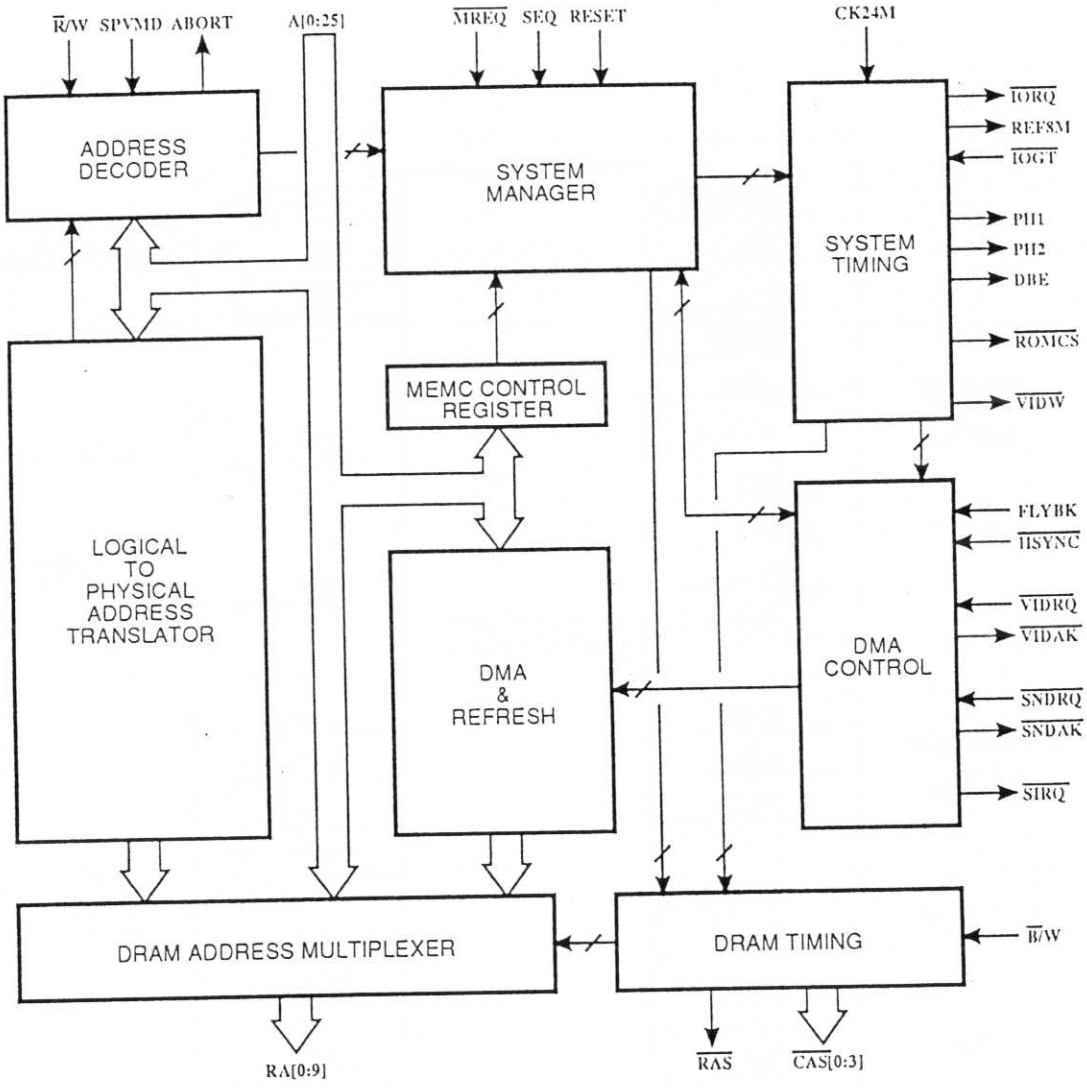
Up to 4MBytes of DRAM may be connected to MEMC, which provides all signals and refresh operations for a wide variety of standard DRAMs. A *Logical to Physical Address Translator* maps the Physical memory into a 32MByte Logical address space (with three levels of protection) allowing Virtual Memory and Multi-Tasking operations to be implemented. Fast "page mode" DRAM accesses are used to maximise memory bandwidth.

MEMC supports Direct Memory Access (DMA) read operations with a set of programmable *DMA Address Generators*, which provide a circular buffer for Video data, a linear buffer for Cursor data, and multiple buffers for Sound data.

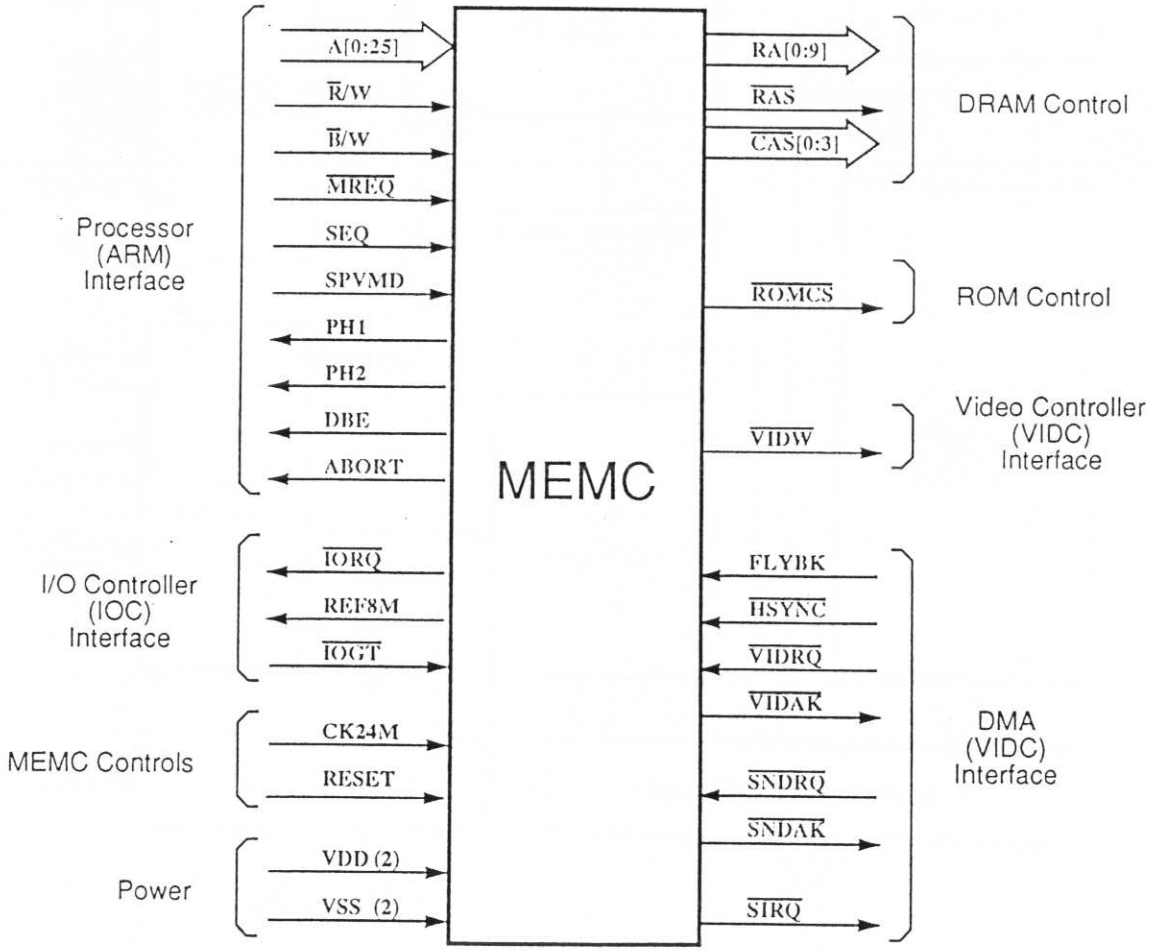
FEATURES

* Directly drives standard Dynamic RAMs
* Supports up to 4MBytes of real memory
* Logical to Physical address translation
* Three protection levels supported
* Uses fast "Page mode" DRAM accesses to maximise memory bandwidth
* Internal DMA address generators for Video, Cursor and Sound data buffers
* Arbitrates memory between the processor and DMA.
* Many ROM speeds supported
* Provides all critical system timing signals, including processor clocks.
* Fabricated in CMOS for low power

2. Block Diagram



3. Functional Diagram



4. Description of Signals

Pin Numbers given for the Jedec B package

Name	Pin	Type	Description
A[0:25]	26-10,8-1,68	IC	Processor address lines.
$\overline{R}$/W	62	IC	Processor Not-Read/Write. Determines the direction of data flow during processor memory accesses. (Note 1)
$\overline{B}$/W	63	IC	Processor Not-Byte/Word. Determines whether a processor memory access is byte-wide (8-bits) or word-wide (32-bits). (Note 1)
$\overline{\text{MREQ}}$	55	IC	Processor memory request. This signal should be set LOW if the processor will be accessing memory in the *next* processor cycle. (Notes 1,2)
SEQ	54	IC	Processor sequential access. This signal should be set HIGH if the *next* processor cycle will access an address sequential to the current address. (Note 2)
SPVMD	52	IC	Supervisor mode select. The MEMC Supervisor protection mode is selected while this line is HIGH. (Note 3)
PH1, PH2	66, 65	OC	Processor clocks. These pins drive the two phase, non-overlapping clock inputs of the ARM processor.
DBE	56	OC	Processor data bus enable. This active HIGH signal enables the processor data bus during processor write cycles, and may be inverted externally to provide an active LOW write enable for the Dynamic RAMs.
ABORT	53	OC	Processor abort. This line is driven HIGH by MEMC to inform the processor that the current memory access is illegal. (Note 1)
$\overline{\text{IORQ}}$	59	OC	Input/Output cycle request. This signal is driven LOW by MEMC to inform the I/O controllers that an IO cycle is being requested by the processor.
REF8M	64	OC	8MHz Reference clock.
$\overline{\text{IOGT}}$	58	IC	Input/Output cycle grant. A LOW on this input informs MEMC that the I/O Controller is ready to complete the IO cycle.
CK24M	67	IC	24MHz Master clock.
RESET	44	IC	Reset input. Active HIGH.
RA[0:9]	28-37	OT	RAM address bus. Multiplexed Row and Column address lines from MEMC which will drive up to 32 DRAMs without external buffers. (Note 4)
$\overline{\text{RAS}}$	38	OT	Row address strobe. The HIGH to LOW transition of $\overline{\text{RAS}}$ strobes the Row address on RA[0:9] into the DRAMs. This line will drive up to 32 DRAMs without external buffers.

$\overline{\text{CAS}}$[0:3]	39-42	OT	Column address strobes. Each line controls a block of 8-bits of memory; one block for each byte of the 4-byte word. The HIGH to LOW transition of a $\overline{\text{CAS}}$[0:3] line strobes the Column address on RA[0:9] into the DRAMs. Each line will drive up to 8 DRAMs without external buffers.
$\overline{\text{ROMCS}}$	60	OC	ROM chip select. This line is driven LOW when the processor accesses the Read Only Memories (ROMs).
$\overline{\text{VIDW}}$	51	OC	Video Controller write strobe. This line is driven LOW while the processor is performing a write operation to the Video Controller.
FLYBK	45	IC	Video vertical flyback. This signal should be set HIGH while the video retrace is in progress. **FLYBK** is used to initialise the video and cursor DMA address pointers.
$\overline{\text{HSYNC}}$	46	IC	Video horizontal synchronisation. Video data requests made while this signal is LOW will obtain data from the cursor data buffer. A video data request made when $\overline{\text{HSYNC}}$ is HIGH obtains data from the video data buffer.
$\overline{\text{VIDRQ}}$	48	IC	Video data request. A LOW on this line requests a video or cursor DMA operation (depending on the sense of $\overline{\text{HSYNC}}$).
$\overline{\text{VIDAK}}$	50	OC	Video data acknowledge. This line is driven LOW to indicate that the requested video/cursor data is being fetched from RAM. The data should be latched on the rising edge of $\overline{\text{VIDAK}}$.
$\overline{\text{SNDRQ}}$	47	IC	Sound data request. A LOW on this line requests a sound DMA operation.
$\overline{\text{SNDAK}}$	49	OC	Sound data acknowledge. This line is driven LOW to indicate that the requested sound data is being fetched from RAM. The data should be latched on the rising edge of $\overline{\text{SNDAK}}$.
$\overline{\text{SIRQ}}$	57	OC	Sound interrupt request. This line is driven LOW to request a sound service interrupt operation from the processor. $\overline{\text{SIRQ}}$ is set LOW on reset.
VSS	27,61	PWR	Ground supply.
VDD	9,43	PWR	Positive supply.

Key to Signal Types:

IC	CMOS compatible input
OC	CMOS compatible output
OT	TTL compatible output
PWR	Power pins

See D.C. Parameters (Section 7).

NOTES:

(1) The word "Memory" in this context refers to any device mapped into the processor's address space.

(2) Some of the processor signals are asserted in the processor cycle preceding that in which they are used.

(3) **SPVMD** is generally connected to the **TRANS** pin of the ARM processor.

(4) The bit order and logic level of the **RA[0:9]** RAM address bus changes according to the *Page size* selected in MEMC. (see Appendix A)

5. General Description

5.1 Protection Modes

MEMC may be operated in three protection modes:

(i) *Supervisor Mode*

Supervisor mode is selected while the **SPVMD** input is held HIGH. This is the most privileged mode, allowing the entire memory map to be freely accessed.

(ii) *Operating System Mode (OS Mode)*

OS mode is selected by setting a control bit in the *MEMC Control Register* (which may only be done from Supervisor mode). OS mode is more privileged than User mode when accessing Logically Mapped RAM, but acts like User mode in all other cases.

(iii) *User Mode*

User mode is the least privileged of the three protection modes. Unprotected pages in the Logically Mapped RAM may be accessed when in User mode, and the ROM space may be read, but no other accesses are allowed.

All attempts to access protected addresses from an insufficiently privileged mode (User mode or OS mode) will activate the **ABORT** line without performing the access.

5.2 Memory Pages

MEMC treats the DRAM it controls as a set of 128 sequential *Physical Pages*. The *Page* is the fundamental unit of memory used by MEMC[1] , and the *Page Size* may be selected as 4, 8 16 or 32 KBytes by programming the *MEMC Control Register*.

The page size selection affects the DRAM address multiplexer, so it is essential to choose the correct page size for the amount of memory being controlled. Table 1 shows the page size selections for most DRAM configurations. When less than 512KBytes of DRAM is connected to MEMC, a page size of 4KBytes should be used, but note that two or more Physical pages will now map onto the same address in the DRAM.

5.3 Memory Map

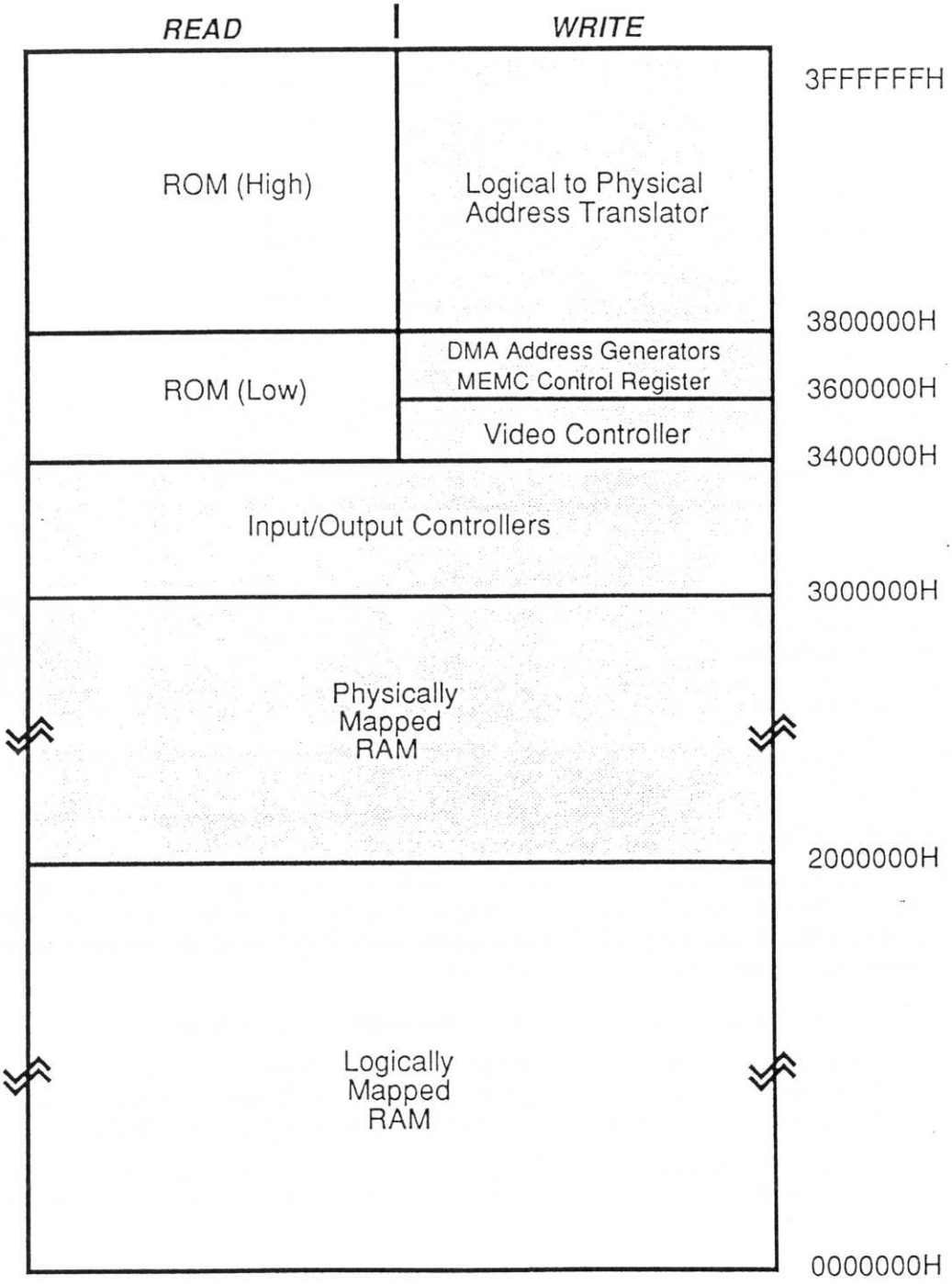
MEMC accepts 26 address lines from the processor, **A[0:25]**, which are decoded as shown by the memory map in Figure 1.

5.3.1 Logically Mapped RAM (Read/Write: 0000000H - 1FFFFFFH)

The bottom 32MBytes of the memory map consists of Logically mapped RAM. MEMC treats this area of the map as a set of contiguous *Logical Pages* (there may be 8192, 4096, 2048 or 1024 Logical pages depending upon the page size selected).

---

[1] *The MEMC Page* unit should not be confused with the "Page mode access" capability of Dynamic RAMS.



NOTE: The shaded areas are only accessible while Supervisor mode is selected.

Figure 1: Processor memory map as decoded by MEMC

Total amount of DRAM	Page Size	Number of Physical Pages	Number of Logical Pages
512 KBytes	4 KBytes	128	8192
1 MByte	8 KBytes	128	4096
2 MBytes	16 KBytes	128	2048
4 MBytes	32 KBytes	128	1024

Table 1: Recommended Page size settings

When a Logical page is accessed, the *Logical to Physical Address Translator* attempts to convert the *Logical Page Number* to a *Physical Page Number*. Provided that the mapping exists, and the request is being made in a sufficiently privileged mode, the appropriate Physical page will be accessed. If the mapping does not exist, or the access is made with insufficient privilege, MEMC will signal the processor by setting the **ABORT** line HIGH, and the DRAM will not be activated.

The Logical to Physical mapping and protection status of each Logical page is undefined at power on, but may be programmed at any time by writing to the *Logical to Physical Address Translator*.

5.3.2 Physically Mapped RAM (Read/Write: 2000000H - 2FFFFFFH)

The Physically mapped RAM occupies 16MBytes of the memory map, and may only be accessed when Supervisor mode is selected. The 128 *Physical pages* appear sequentially in this area of the map, with the RAM image being repeated after every 128th page (so that, with a page size of, say, 8KBytes, the entire 1MByte of RAM would occur 16 times throughout this area).

5.3.3 Input/Output Controllers (Read/Write: 3000000H - 33FFFFFH)

This area of the map is reserved for I/O Controllers (including IOC). When a Supervisor mode access is made in this memory range, MEMC asserts $\overline{\text{IORQ}}$ (IO cycle request), and stops the processor clocks. The IO cycle terminates after both $\overline{\text{IORQ}}$ and $\overline{\text{IOGT}}$ are seen LOW on the rising edge of **REF8M**.

NOTE: Care must be taken not to access a non-existent I/O Controller, otherwise MEMC will wait indefinitely for an active $\overline{\text{IOGT}}$ signal that never appears, and the processor will stop until **RESET** is asserted.

5.3.4 ROM (Read: 3400000H - 3FFFFFFH)

Read Only Memory may be read freely from any protection mode. The ROM space is divided into two areas:

(i) Low ROM (4MBytes from 3400000H to 37FFFFFH)

(ii) High ROM (8MBytes from 3800000H to 3FFFFFFH)

The two ROM areas are distinguished only by the fact that each may be programmed to operate at its own speed. This would allow the High ROM area to contain fast system ROMs, with slower applications ROMs in the Low ROM area.

The ROM speeds default to the slowest setting when **RESET** is asserted, and may be altered by reprogramming the *MEMC Control Register* .

5.3.5 Video Controller (Write: 3400000H - 35FFFFFH)

A write operation made anywhere in the Video Controller space (while MEMC is in Supervisor mode) activates the $\overline{\text{VIDW}}$ output from MEMC.

5.3.6 Address Generators & Control Register (Write: 3600000H - 37FFFFFH)

This address space decodes to some of MEMC's internal registers. The *DMA Address Generators* supply the Physical RAM address used to obtain data during Video, Cursor and Sound Direct Memory Access operations, and the *MEMC Control Register* controls a number of the functions of MEMC.

The processor data bus is not connected to MEMC; instead, the internal registers are programmed by encoding the data in the address bus, and performing a write operation with MEMC in Supervisor mode.

5.3.7 Logical to Physical Address Translator (Write: 3800000H - 3FFFFFFH)

The mapping of *Logical pages* to *Physical pages*, and protection mode associated with each mapping, may be controlled by programming the *Logical to Physical Address Translator*. The Address Translator is programmed by encoding data in the address lines, and performing write operations in Supervisor mode to this area of the memory map.

5.4 Effect of Reset

When the **RESET** line is taken HIGH, MEMC initialises to the following state:

- Memory Map

  The ARM processor starts executing code from location 0000000H after **RESET** goes inactive. To ensure that the processor always finds valid code at this location (which is normally Logically mapped RAM), MEMC continually enables ROM.

  To restore the normal memory map, the processor must first perform a memory access with the address lines A[25] and A[24] both LOW, and then perform a memory access with address line A[25] HIGH. These conditions are satisfied when the processor starts executing instructions from location 0000000H, and later jumps to the normal ROM space.

  Note that a processor write operation should not be performed while ROM is continually enabled, or a data bus clash will occur.

- ROM access times

  The ROM access times for both High and Low ROM are reset to 450ns.

- Page sizes

  The DRAM page size defaults to 4KBytes.

- Operating System mode

  The Operating System mode is disabled.

- Direct Memory Access (DMA) operations

  Sound DMA operations are disabled. Video and Cursor DMA operations are unaffected by reset.

- Sound Interrupts

  The Sound Interrupt pin, $\overline{\text{SIRQ}}$ is set LOW. The interrupt may be removed by initialising the Sound DMA buffers in the *DMA Address Generators*. (see Section 6.7.3)

- IO cycle request

  The $\overline{\text{IORQ}}$ line is held HIGH during reset to avoid accidentally triggering an I/O Controller if the processor generates spurious addresses while **RESET** is active.

- Test mode

  The *Test mode* is disabled by **RESET**. Test mode is only used for functional testing of MEMC out of the system.