IOC Datasheet

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Contents

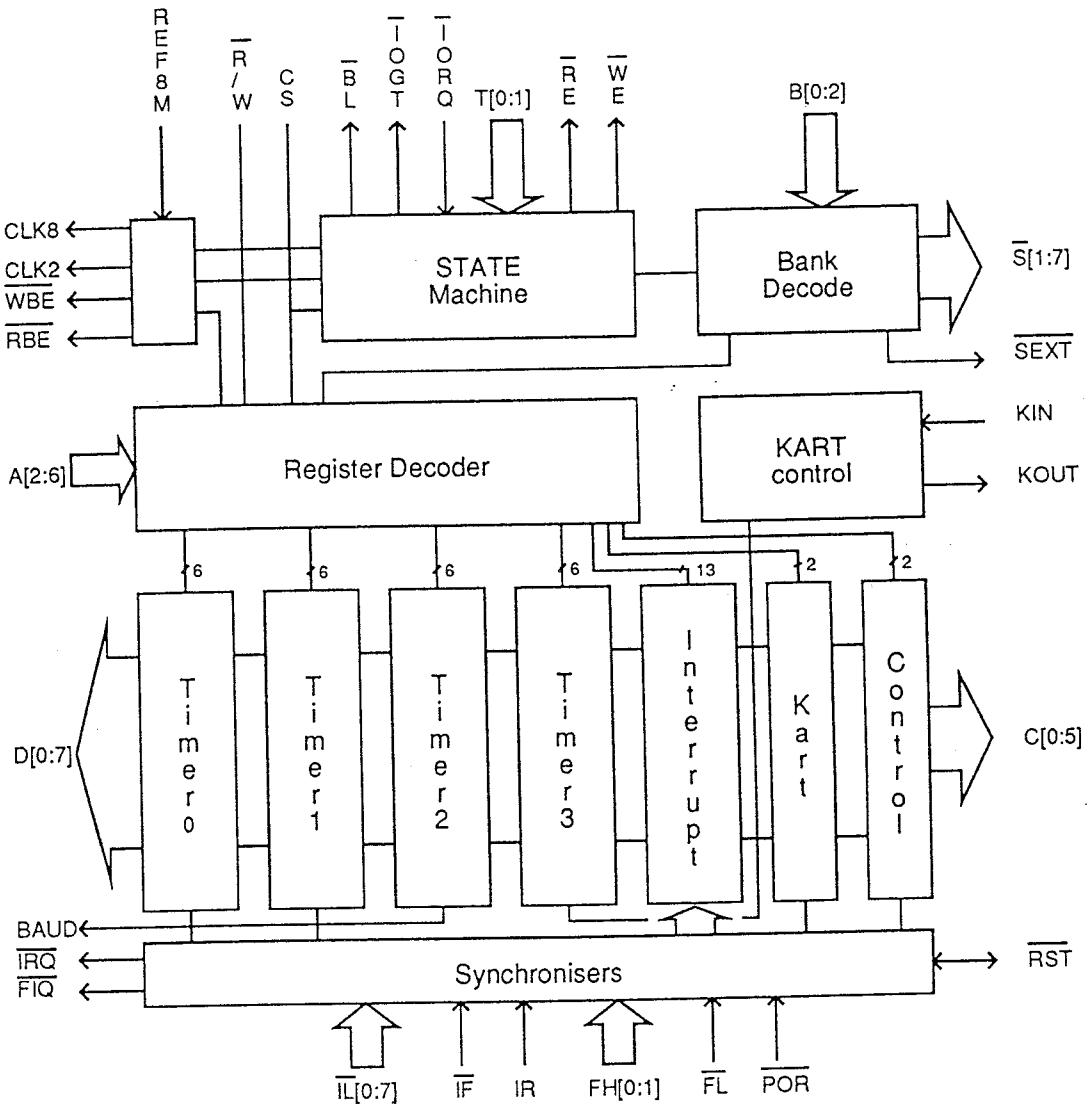
1. Introduction

The Input Output Controller (IOC) is a member of the Acorn RISC Machine (ARM) support chip set, and interfaces directly with the Memory Controller (MEMC) and the Video Controller (VIDC) to provide a unified view of interrupts and peripherals within an ARM based system. IOC manages an 8 to 32 bit IO data bus to which peripheral controllers may be connected, provides a set of internal functions, and controls the access cycles to the external peripherals. The internal functions include timers, a serial keyboard interface, and interrupt control logic to satisfy the basic requirements of a computer system. The peripheral timing cycles allow standard peripheral controllers from a wide range of manufacturers to be interfaced without any additional logic. A flexible control port offers a number of general purpose input/output pins.

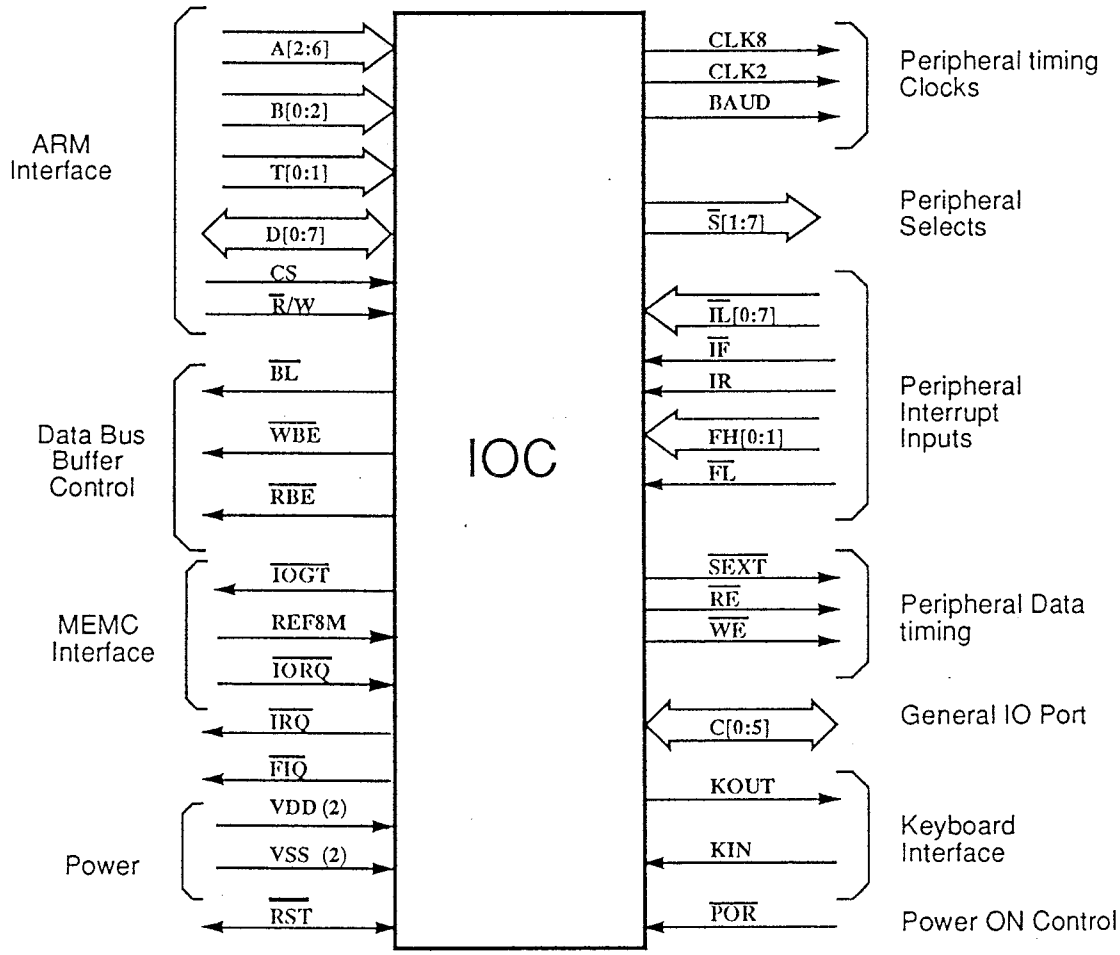
FEATURES

* Power-on Reset Control
* 4 independent 16 bit programmable counters
* Bi-directional serial keyboard interface
* 6 Programmable bi-directional control pins
* Interrupt mask, request and status registers for $\overline{\text{IRQ}}$ and $\overline{\text{FIQ}}$
* 14 level-triggered interrupt inputs
* 2 edge-triggered interrupt inputs
* 4 programmable peripheral cycles
* 7 external peripheral selects
* ARM/IO bus interface control
* Expansion bus buffer control
* Fabricated in CMOS for low power consumption

2. Block diagram



3. Functional Diagram



4. Description of Signals

Name	Pin	Type	Description
REF8M	8	IC	8 MHz reference clock. The timings of all interface signals to ARM and MEMC are referenced to this clock.
CLK8	54	OC	8 MHz clock for external peripherals. This is **REF8M** buffered and inverted.
CLK2	2	OC	2 MHz clock for external synchronous peripheral timing.
$\overline{\text{IORQ}}$	7	IC	IO cycle request. A LOW on this input indicates that the ARM is performing an IO cycle.
$\overline{\text{IOGT}}$	6	OD	IO cycle grant. An IO cycle is complete cycle when $\overline{\text{IOGT}}$ and $\overline{\text{IORQ}}$ are both LOW on a rising edge of **REF8M**.
$\overline{\text{BL}}$	5	OD	Buffer latch control for the ARM/IO data.
D[0:7]	18-25	IOCZ	Bi-directional 3-state data bus for accesses to the internal registers.
$\overline{\text{RBE}}$	11	OC	Read Buffer Enable. This is taken LOW during a read of any IO Controller or peripheral.
$\overline{\text{WBE}}$	12	OC	Write Buffer Enable. This is taken LOW during a write to any IO Controller or peripheral.
$\overline{\text{SEXT}}$	55	OC	Select external peripheral. This may be used to control an optional external data buffer which may be placed between IOC and the IO bus if the bus is heavily loaded . It is active for any IOC peripheral access.
T[0:1]	1,68	IC	Type lines. These are used to specify the timing characteristics of any peripheral access.
$\overline{\text{R}}$/W	10	IC	Not read/write. This line determines the direction of data transfer in an IO cycle: LOW to read or HIGH to write an IO device.
B[0:2]	64-66	IC	Bank select lines. These are used to select an IO access either to an internal IOC register (B[0:2]=0) or to a peripheral (B[0:2]>0). B[0:2]are decoded to drive one of the peripheral select lines, $\overline{\text{S[1:7]}}$, LOW.
$\overline{\text{S[1:7]}}$	63-61,59-56	OC	Active low peripheral selects which indicate valid address and write data. They are decoded from B[0:2]
CS	67	IC	Chip select. When HIGH allows internal register and peripheral accesses to be performed. Even when LOW, IOC continues to control the **RBE** and **WBE** lines.
A[2:6]	13-17	IC	Address lines for selecting internal registers.
$\overline{\text{RE}}$	4	OC	Read enable, used to time peripheral read accesses.
$\overline{\text{WE}}$	3	OC	Write enable, used to time peripheral write accesses.
$\overline{\text{IRQ}}$	51	OD	Interrupt request to ARM.
$\overline{\text{FIQ}}$	50	OD	Fast Interrupt request to ARM.
$\overline{\text{IL[0:7]}}$	33-40	IT	IRQ interrupt active low inputs.

$\overline{IF}$	41	IT	IRQ interrupt active falling-edge input.
IR	42	IT	IRQ interrupt active rising-edge input.
FH[0:1]	30-31	IT	FIQ interrupt active high inputs.
$\overline{FL}$	32	IT	FIQ interrupt active low input.
C[0:5]	44-49	IOD	Control pins. A bi-directional programmable open-drain port.
BAUD	27	OC	Baud rate generator output.
KIN	52	IT	Keyboard Serial interface input.
KOUT	53	OC	Keyboard Serial interface output.
$\overline{POR}$	28	IS	Power-on reset input, usually connected to an external RC network. It is used to generate a reset pulse at power-on and to differentiate power-on from subsequent causes of reset.
$\overline{RST}$	29	IOD	The reset line is driven low by $\overline{POR}$ at power-on and may be driven low externally at any time.
VSS	9,43	PWR	Ground supply
VDD	26,60	PWR	Positive supply

Key to Signal Types

IC	Input CMOS compatible
IT	Input TTL compatible
IS	Input with Schmitt trigger
OC	Output CMOS compatible
OD	Output open-drain
IOD	Bi-direction open-drain
IOCZ	Bi-directional 3-state
PWR	Power pins

5. Programming Model

If the Bank B[0:2], Type T[0:1], Chip Select CS and Addresses Lines A[2:6] of IOC are joined to the CPU address lines, the IOC and peripherals are viewed as memory mapped devices. This allows the programmer to specify in a single memory instruction the peripheral to be accessed and the type of timing cycle it requires. In a typical system as shown in figure 1 the **IO Controller** space is devided into two halves. The upper half is occupied by IOC, and the lower half is left for additional **IO Controllers.**

The IOC space is decoded into eight banks, bank zero through seven, by the B[0:2] lines. The bottom bank, bank zero, maps to the internal registers of IOC. The remaining seven banks map to the seven peripheral select lines $\overline{S[1:7]}$ respectively. The seven peripheral banks are each further decoded into four types of peripheral access by the T[0:1] lines. (See figure 2.) The type of the peripheral access determines the timing of the data transfer cycle.

A particular peripheral device may be accessed by choosing an address where CS is HIGH, B[0:2] decodes to the appropriate peripheral select, and T[1:0] selects a cycle with timing to suit the accessed device. The remaining low order address lines may be used to select the register within the device.

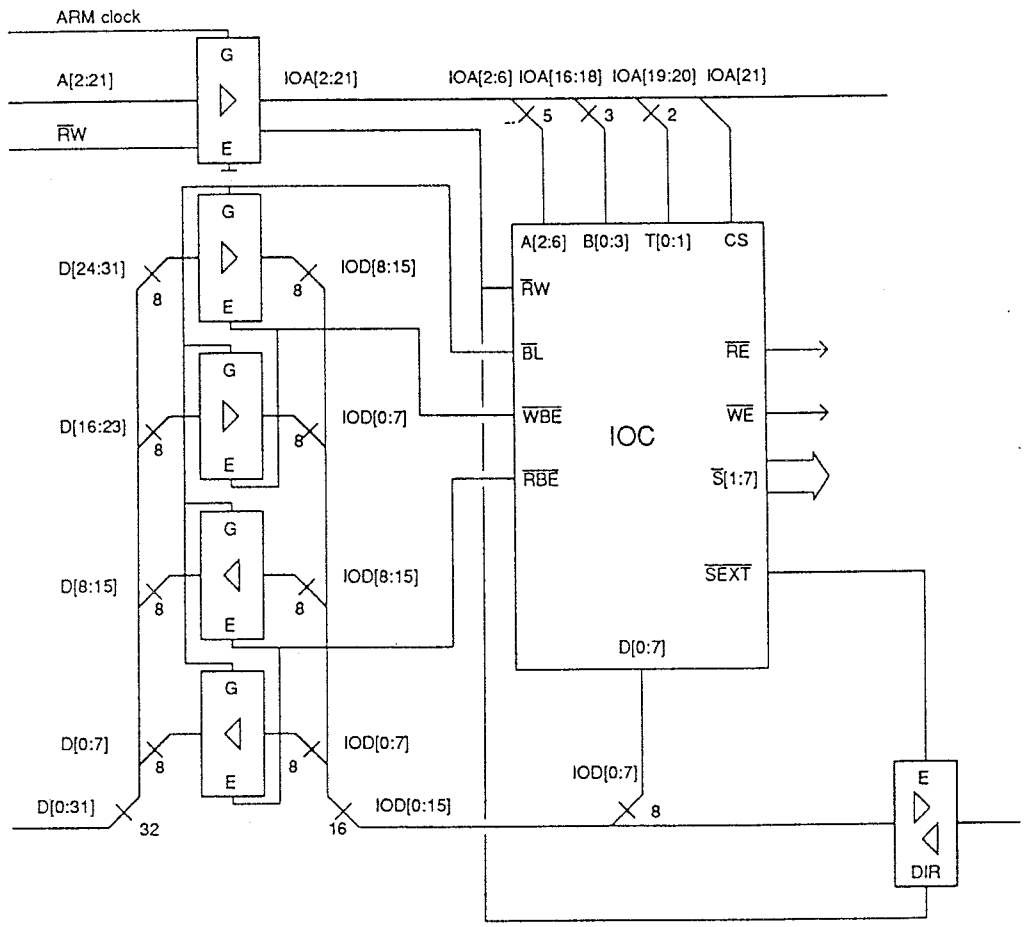


Figure 1: Typical system

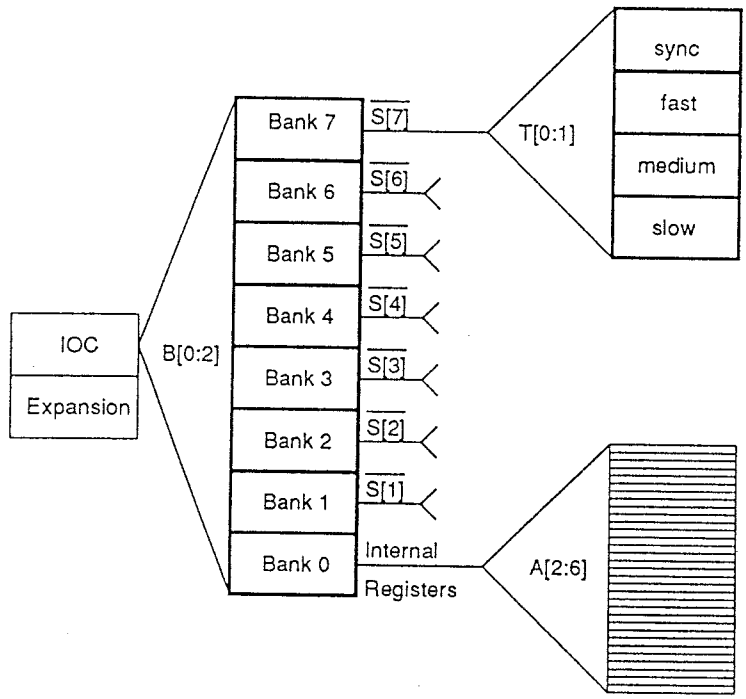


Figure 2: Typical Decoding Structure

5.1 Access Speed

While the peripherals appear as memory mapped devices, it is not possible for accesses to them to be completed in the same time as accesses to main memory. Four different access cycle timings are available, and the timing for an access is determined from the state of T[0:1] at the start of the access.

5.2 Addresses

The pipelined ARM addresses are latched by external buffers to provide valid signals thoughout both IO accesses and ROM reads. The latches are controlled by an ARM clock line which is stretched during slow cycles.

5.3 Data

The ARM data bus is connected to the IO data bus by a set of latches. These provide two functions. Firstly they isolate the IO bus load from the main data bus, and secondly they allow for the mis-match in speed between the two buses. These buffers are controlled by the $\overline{BL}$, $\overline{RBE}$ and $\overline{WBE}$ lines from IOC .

6. Internal Registers

All internal registers are accessed with no wait states, and accesses take two **REF8M** cycles to complete. The internal registers are decoded as bank zero, so to access them the **B[0:2]** lines must all be LOW and the **IOC** must be selected by taking **CS** HIGH. The individual registers are then addressed using the **A[2:6]** lines. The registers are decoded on word boundaries. The state of the **T[0:1]** lines is ignored.

Addr.	Read	Write
00H	Control	Control
04H	Serial Rx Data	Serial Tx Data
08H	-	-
0CH	-	-
10H	IRQ status A	-
14H	IRQ request A	IRQ clear
18H	IRQ mask A	IRQ mask A
1CH	-	-
20H	IRQ status B	-
24H	IRQ request B	-
28H	IRQ mask B	IRQ mask B
2CH	-	-
30H	FIQ status	-
34H	FIQ request	-
38H	FIQ mask	FIQ mask
3CH	-	-
40H	T0 count Low	T0 latch Low
44H	T0 count High	T0 latch High
48H	-	T0 go command
4CH	-	T0 latch command
50H	T1 count Low	T1 latch Low
54H	T1 count High	T1 latch High
58H	-	T1 go command
5CH	-	T1 latch command
60H	T2 count Low	T2 latch Low
64H	T2 count High	T2 latch High
68H	-	T2 go command
6CH	-	T2 latch command
70H	T3 count Low	T3 latch Low
74H	T3 count High	T3 latch High
78H	-	T3 go command
7CH	-	T3 latch command

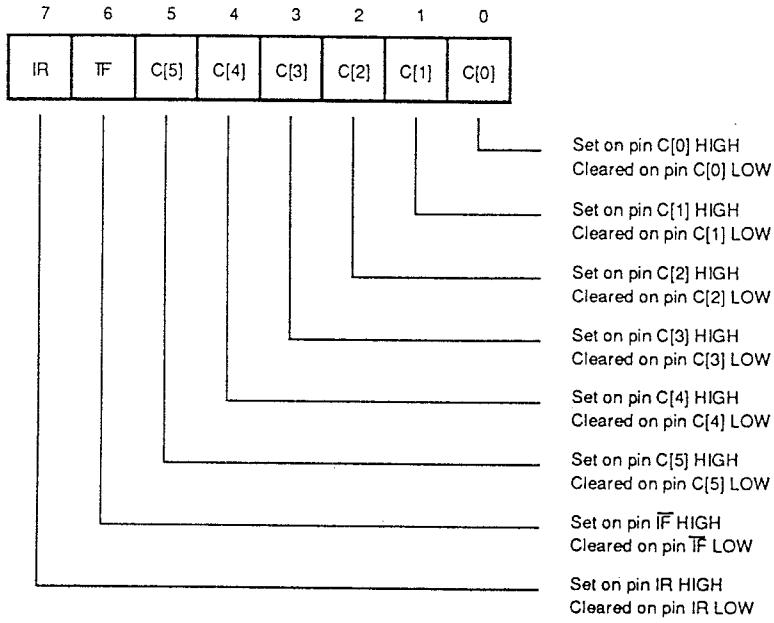
Table 1: Internal register memory map

6.1 Control Register

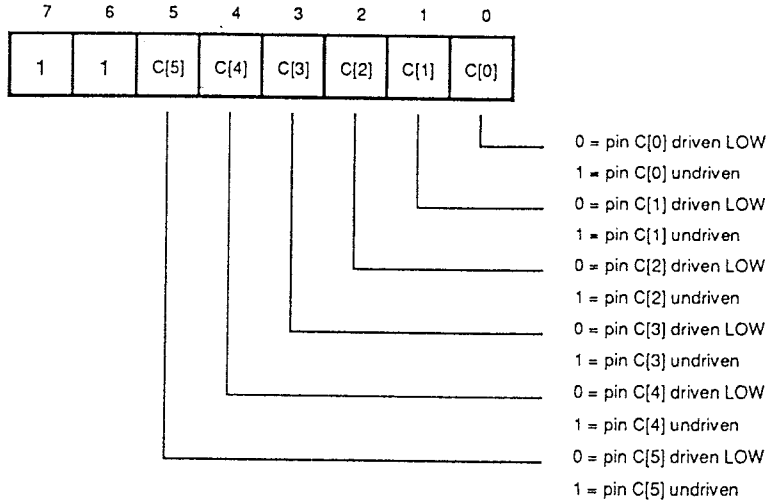
The *control register* allows the external control pins C[0:5] to be read and written and the status of the IR and $\overline{IF}$ inputs to be inspected. The C[0:5] bits manipulate the C[0:5] IO Port. When read, they reflect the current state of these pins. When written LOW the output pin is driven LOW. These outputs are open-drain, and if programmed HIGH the pin is undriven and may be treated as an input.

On reset all bits in the *control register* are set to "1".

6.1.1 Control register 00H read



6.1.2 Control register 00H write



6.2 Keyboard Asynchronous Receiver Transmitter (KART)

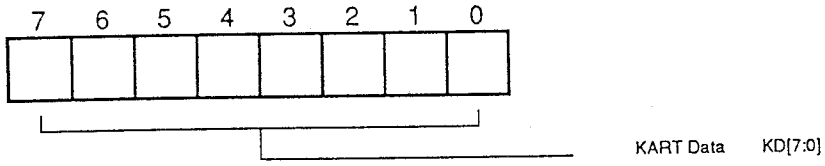
The KART provides an asynchronous serial link, usually to a keyboard. It is of fixed format with 8 bits to a character which is framed with one start bit and two stop bits. The least significant bit *KD[0]* is transmitted/received first. The KART divides into two halves, the receiver and the transmitter.

The ARM accesses the receiver via the *Serial Rx Data register*. A clock of 16 times the data rate is used by the KART to clock in the serial data from the **KIN** pin. When a data byte has been received, the *SRx* bit is asserted in the *IRQ Status B Register* to indicate that the byte is available for reading. False start bits of less than a half bit duration are ignored.

The ARM accesses the transmitter via the *Serial Tx Data register*. The byte written to the *Serial Tx Data register* is transmitted serially from the **KOUT** pin, and the *STx* bit is asserted in the *IRQ Status B register* to indicate that the transmission is finished and the *Serial Tx Data register* may be reloaded.

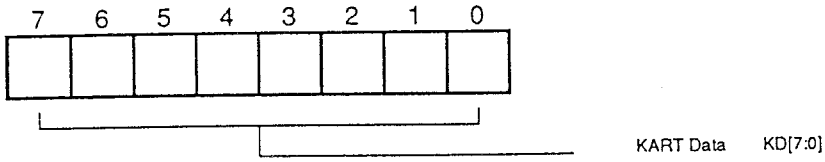
The receive and transmit speeds are the same and are programmed using *counter 3*.

6.2.1 Serial Tx Data register 04H write



Writing to this register loads the serial output shift register, clears any outstanding *TRx* interrupt and starts the transmission. An interrupt is raised when the register is ready to be reloaded.

6.2.2 Serial Rx Data 04H read



Reading from this register clears any outstanding *SRx* interrupt and returns the currently received byte. Data is only valid while the *SRx* bit is set in the *IRQ status B register*.

6.2.3 Initialisation

After Power-On, the KART is in an undefined state. The KART is initialised by programming the serial line speed using *counter 3* and performing a read from the *Serial Rx Data register*, discarding the data byte. This will clear any outstanding receive interrupt and enable the KART for the next reception. Finally the *Tx Data register* should be written to. This will abort any transmission in progress, cause a new one to be started, and clear any *STx* interrupt.

6.2.4 Receive Interrupt

The *SRx* interrupt is set halfway though the reception of the last data bit. Care should be taken to ensure that the last bit has been received before the *Serial Rx data register* is read, to prevent this bit being interpreted as the start bit of the next packet.

6.3 Interrupt Registers

The IOC generates two independant interrupt requests, $\overline{\text{IRQ}}$ and $\overline{\text{FIQ}}$. Interrupt requests can be caused by events internal to IOC or by external events on the interrupt or control port input pins.

The IOC interrupts are controlled by four types of register, *status*, *mask*, *request* and *clear*. The *status registers* reflect the current state of the various interrupt sources. The *mask registers* determine which sources may generate an interrupt. The *request registers* are the logical AND of the *status* and *mask registers* and indicate which sources are generating interrupt requests to the processor. The *clear register* allows clearing of interrupt requests where appropriate. The *mask registers* are undefined after power up.

The *IRQ* events are split into two sets of registers *A* and *B* . There is no priority encoding of the sources.

6.3.1 Internal Interrupt Events

* Timer interrupts *TM[0:1]*.
* Power-on reset $\overline{POR}$.
* Keyboard Rx data available *SRx*.
* Keyboard Tx data register empty *STx*.
* Force interrupts *"1"*.

6.3.2 External Interrupt Events

* IRQ active low inputs $\overline{IL[0:7]}$.
* IRQ falling-edge input $\overline{IF}$.
* IRQ rising-edge input *IR*.
* FIQ active high inputs *FH[0:1]*.
* FIQ active low input $\overline{FL}$.
* Control port inputs *C[3:5]*.

6.3.3 Level Interrupts

The majority of external and a few of the internal interrupt sources are level sensitive. When one of these sources has caused an interrupt it is cleared by removing the source.

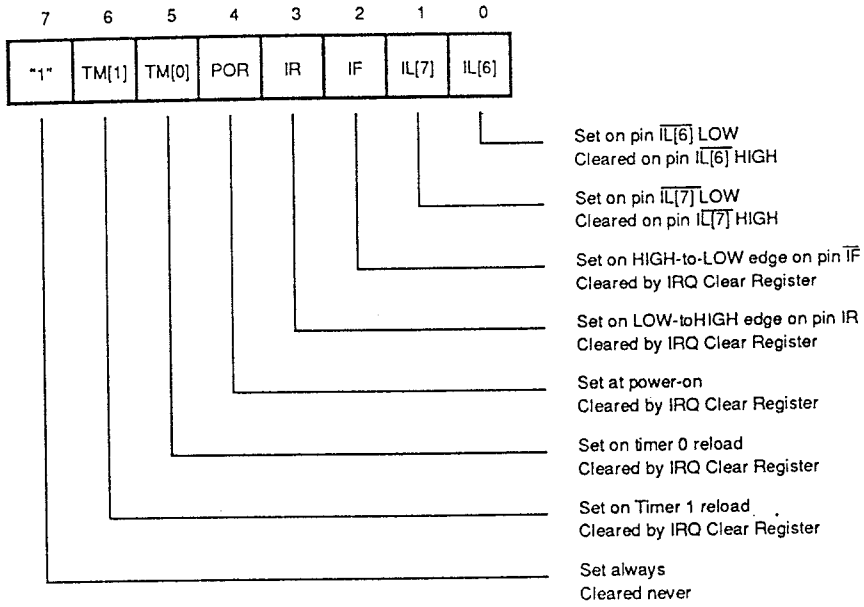
6.3.4 Latched Interrupts

The $\overline{\text{IF}}$, IR, $\overline{\text{POR}}$ and TM[0:1] sources are latched. That is, once one of these sources has caused an interrupt, it must be cleared by an explicit write of "1" to the appropriate bit in the *IRQ Clear A register*. One or many may be cleared in a single operation.

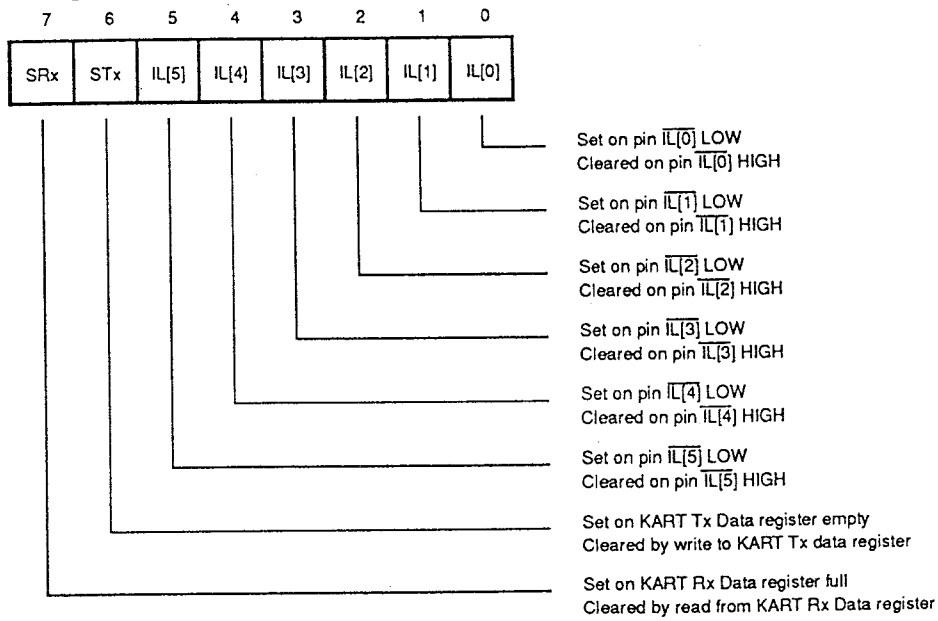
6.3.5 Synchronisation

All the interrupt sources are synchronised by the REF8M clock input. It can take up to three clock phases before a source is recognised as requesting an interrupt, and the same delay occurs between a level sensitive request going inactive at an input pin and the removal of the corresponding bit from the *status register* and the processor interrupt line.

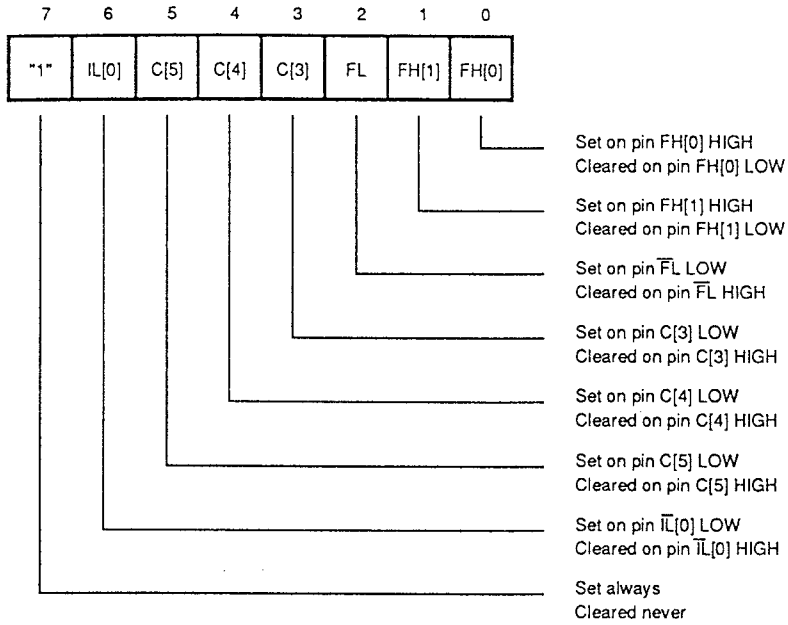
6.3.6 IRQ Status A register 10H read



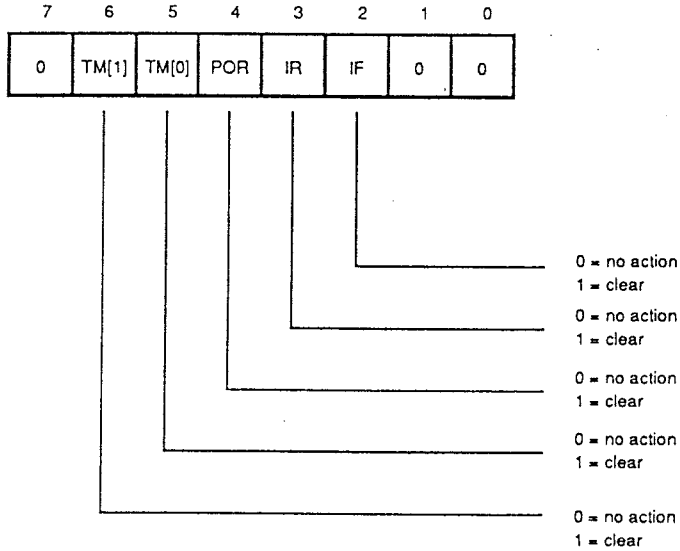
6.3.7 IRQ Status B register 20H read



6.3.8 FIQ Status register 30H read



6.3.9 IRQ Clear register 14H write



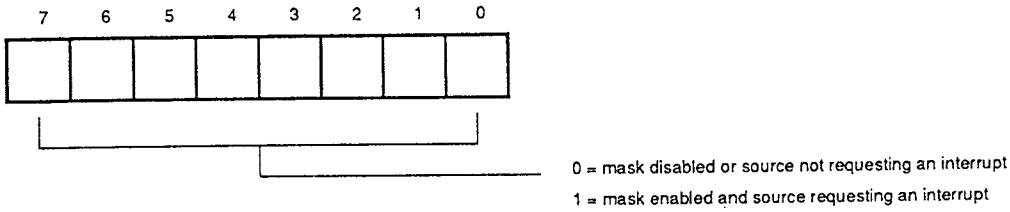
6.3.10 Interrupt Request registers 14H 24H 34H read

These registers show which interrupt sources are currently enabled and active. They give the logical AND of the corresponding *status* and *mask* registers.

(i) IRQ request A address 14H

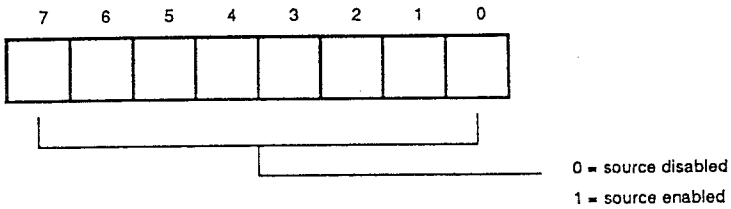
(ii) IRQ request B address 24H

(iii) FIQ request address 34H



6.3.11 Interrupt Mask registers 18H 28H 38H read/write

The *mask registers* are readable to simplify the sharing of these registers between a number of interrupt handlers.



(i) IRQ mask A address 18H

(ii) IRQ mask B address 28H

(iii) FIQ mask address 38H

6.4 Counters

Four identical 16 bit counters are provided. Two are used as timers, the third for the keyboard BAUD rate and the fourth as a general purpose output. They all have fully programmable start/reload values.

Each counter consists of a 16 bit down counter, a 16 bit input latch (*latch low* and *latch high*) and a 16 bit output latch (*count low* and *count high*) which contains the value of the counter when the *latch command* is given. The counter decrements continuously, clocked at 2 MHz. When it decrements to zero, it is reloaded from the *input latch* and recommences decrementing. The reload is used to trigger different events depending on the use of the counter. If a counter is loaded with zero it continuously reloads and does not count. If the *GO register* is written at the same time as the counter reloads an extra 2 MHz clock tick is taken to reload. After power-on the state of the counters is unknown.

latch = *latch low* + 256 * *latch high*

6.4.1 Register actions

Latch low	Writing to this updates the low order byte of the *input latch*
Latch high	Writing to this updates the high order byte of the *input latch*
GO command	Writing to this causes the counter to be reloaded immediately with the *latch* value.
Count low	This causes the low order byte of the output latch to be read.
Count high	This causes the high order byte of the output latch to be read.
Latch command	This causes the current value of the counter to be placed in the output latch.

6.4.2 Counter schematic

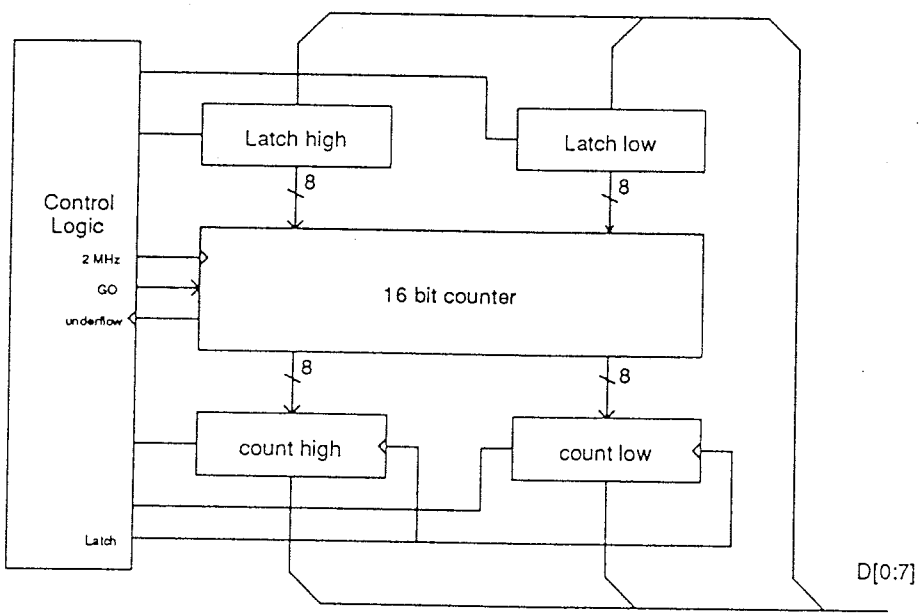


Figure 3: Counter schematic

6.4.3 Counter Registers

	Address for counter				read or
	0	1	2	3	write
Latch low	40H	50H	60H	70H	write
Latch high	44H	54H	64H	74H	write
GO command	48H	58H	68H	78H	write
Count low	40H	50H	60H	70H	read
Count high	44H	54H	64H	74H	read
Latch command	4CH	5CH	6CH	7CH	write

6.4.4 Counters 0 and 1

Two general purpose timers are provided. The reload event sets a timer interrupt, *TM[0:1]* in the *IRQ status A register*. The interrupt is cleared via the *IRQ Clear A register*. In order to generate an interrupt after time, $T_{interval}$, the 16 bit value, *(latch)*, to be used is calculated from the following equation.

$$T_{interval} := latch/2 \quad \mu seconds$$

6.4.5 Counter 2 (BAUD)

The counter 2 output is used to drive the **BAUD** pin. The reload event toggles the BAUD clock line. In order to generate a clock of frequency f_{BAUD}, the 16 bit value, *(latch)*, to be used is calculated from the following equation.

$$f_{BAUD} := 1/(latch+1) \text{ MHz}$$

The maximum BAUD rate of 500kHz is obtained by programming *latch*=1.

6.4.6 Counter 3 (KART)

This counter 3 output controls the speed of the keyboard serial link. In order to generate a baud rate k_{BAUD}, the 16 bit value, *(latch)*, to be used is calculated from the following equation.

$$k_{BAUD} := 1/((latch+1)*16) \text{ MHz}$$

The maximum baud rate of 31250Hz is obtained by programming *latch*=1.

7. Peripherals

The IOC provides control for external peripherals which cannot be accessed in a single cycle. A number of differently timed cycles, selected by the **T[0:1]** lines, are provided. The peripheral cycles are controlled by a state machine clocked from **REF8M** . The cycles are timed to two clocks **CLK2** and **CLK8**. Two timed data strobes, write enable $\overline{WE}$ and read enable $\overline{RE}$, manipulate data.

(Internal accesses complete in two **REF8M** cycles, and the state machine remains IDLE during these.)

The number of **REF8M** cycles an IO access takes to complete depends on three things:

(1) The minimum time for the cycle;

(2) The synchronisation time

(3) DMA activity on the ARM bus.

The times are expressed as in **REF8M** cycles. The first three cycles share common timing and are of fixed duration. The last is synchronised to the **CLK2** output, a 2 MHz square wave. Examples of the peripheral access are given in Appendix A.

T[1:0]	Name	Minimum time (REF8M cycles)	Synchronisation time (REF8M cycles)
0:0	slow	7	0
0:1	medium	6	0
1:0	fast	5	0
1:1	sync	5	0,1,2,3

Table 2: Cycle timing

8. ARM/IO Interface

8.1 Peripheral Address and Data

The peripheral address and data are not provided by IOC, so their timing is system dependent. The following explanations assume that the configuration is as in figure 1. Additionally, process dependent delays though IOC can be up to half a REF8M clock pulse, so there can be considerable skew between signals coming from IOC and those from other sources.

8.1.1 Peripheral Write Cycles

Since the MEMC may perform DMA transfers on the main data bus while an IO cycle is in progress, the write data must be latched to provide valid data throughout the IO cycle. This is done by taking $\overline{BL}$ LOW at the start of the cycle. It is taken HIGH again at the end of the cycle.

8.1.2 Peripheral Read Cycles

To provide fixed duration cycles for the peripherals, the read data is latched by taking $\overline{BL}$ LOW as the $\overline{RE}$ strobe is taken HIGH. This allows the peripheral cycle to complete independently of the processor, and the data is held in the data latches until the processor is ready to complete the IO cycle.

8.2 Peripheral Select Lines

The peripheral select lines $\overline{S[1:7]}$ are timed at the start of a cycle from $\overline{IORQ}$ and disabled at the end of the cycle by the state machine.

8.3 Multiple IO Controllers

The IOC has been designed to allow multiple $\overline{IORQ}$/ $\overline{IOGT}$ devices to be connected to MEMC. For this reason the $\overline{IOGT}$ and $\overline{BL}$ lines are open drain outputs. Even when IOC is not selected it continues to control the external buffer enables $\overline{RBE}$ and $\overline{WBE}$, so additional IO Controllers need not generate these signals.

8.4 IO Grant Line

In order for an internal register access to complete in two REF8M clock cycles the $\overline{IOGT}$ line cannot be made to depend logically on $\overline{IORQ}$, which indicates the start of an IO cycle, as $\overline{IORQ}$ becomes valid too late. Therefore $\overline{IOGT}$ is generated from $\overline{B[0:2]}$ and CS only, and will sometimes be driven LOW during non-IO cycles.

For peripheral access the $\overline{IOGT}$ line is controlled by the state machine.

9. Reset and Power-on

The IOC may be reset in two ways: by driving the bidirectional $\overline{\text{RST}}$ line LOW, or by driving the $\overline{\text{POR}}$ line LOW. The $\overline{\text{POR}}$ pin is designed to be connected to an external RC network to ensure that when power is first applied to the IOC, a system reset signal is generated on $\overline{\text{RST}}$. $\overline{\text{POR}}$ causes an internal latched interrupt to be set to allow system software to differentiate between "power-on" and "soft" resets, and ensures that peripheral chips have had a stable clock for a suitable length of time before being released from reset.

The control register is initialised on reset causing the C[0:5] pins to be set to a known state, HIGH, before the processor commences execution.

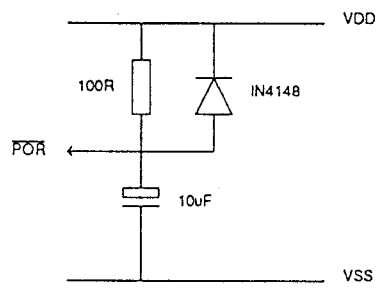


Figure 4: Suggested circuit for power-on reset

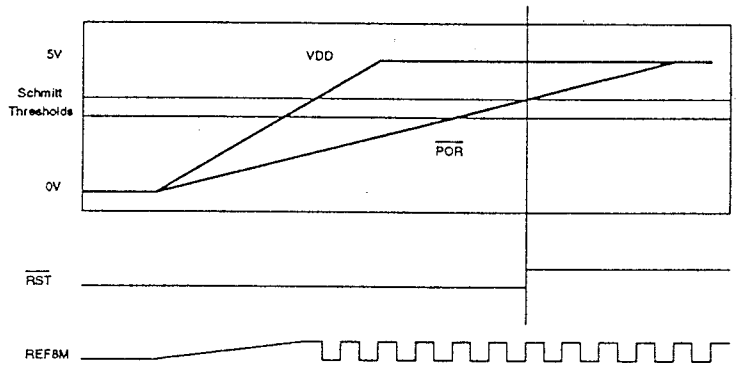
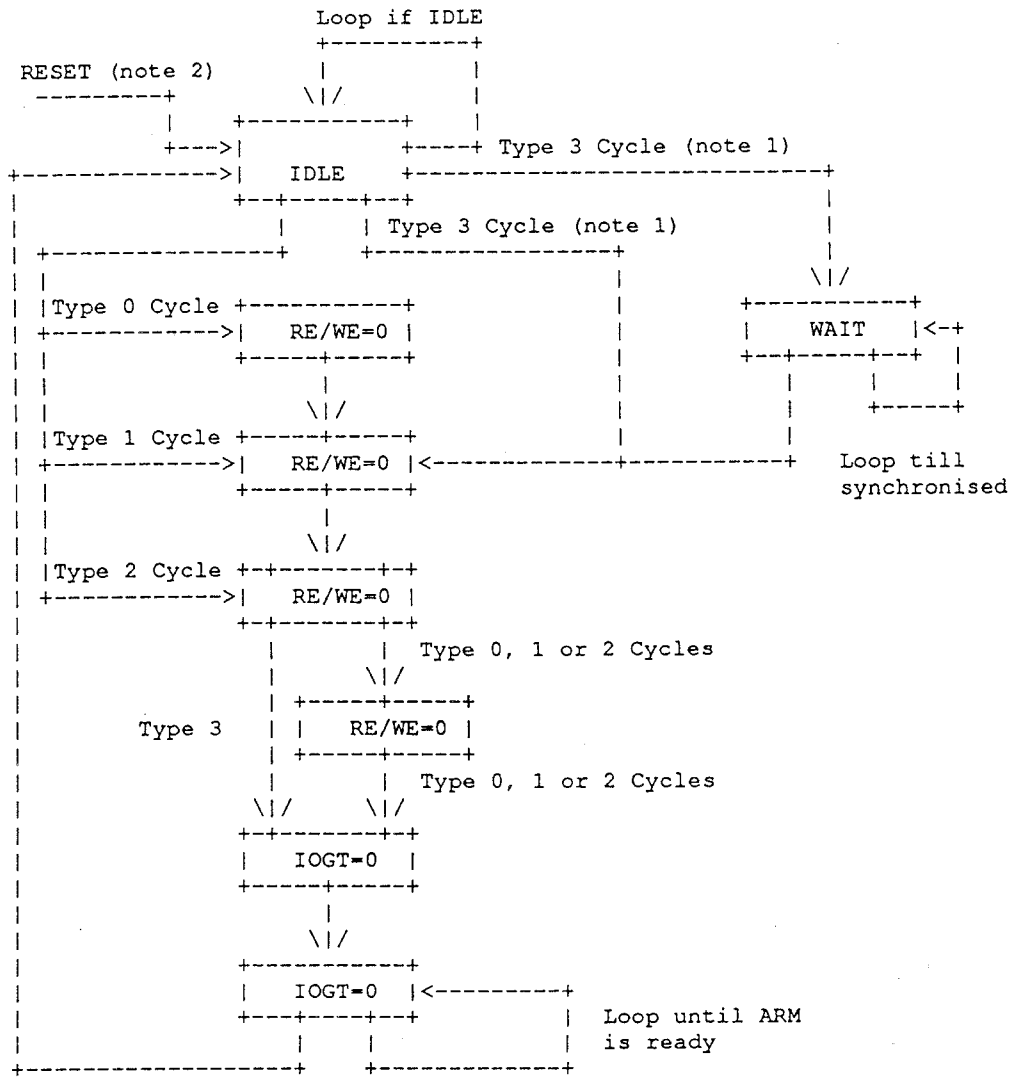


Figure 5: Power-on timing

10. IO-Cycle State Machine



NOTES:

(1) Type 3 cycles will go into the wait state unless the cycle starts at the optimal point in the CLK2 cycle.

(2) RESET is a forcing signal to return to IDLE from any state.

11. DC Parameters

11.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD	Supply voltage	VSS-0.3	VSS+7.0	V	1
Vip	Voltage applied to any pin	VSS-0.3	VDD+0.3	V	1
Ts	Storage temperature	-40	125	deg.C	1

NOTE:

(1) These are stress ratings only. Exceeding the absolute maximum ratings may permanantly damage the device. Operating the device at absolute maximum ratings for extended periods may affect device reliability.

11.2 DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD	Supply voltage	4.75	5.0	5.25	V	
Vihc	IC input HIGH voltage	3.5		VDD	V	1,2
Vilc	IC input LOW voltage	0.0		0.8	V	1,2
Viht	IT input HIGH voltage	2.4		VDD	V	1,3
Vilt	IT input LOW voltage	0.0		0.8	V	1,3
Vihz	IOCZ input HIGH voltage	2.4		VDD	V	1,4
Vilz	IOCZ input LOW voltage	0.0		0.8	V	1,4
Vihd	IOD input HIGH voltage	2.4		VDD	V	1,5
Vild	IOD input LOW voltage	0.0		0.8	V	1,5
Ta	Ambient operating temperature	0		70	deg.C	

NOTES:

(1) Voltages measured with respect to VSS.

(2) IC - CMOS compatible inputs.

(3) IT - TTL compatible inputs.

(4) IOCZ - Bi-directional 3-state inputs.

(5) IOD - Bi-directional open-drain inputs.

11.3 DC Characteristics

KEY

Mes - Values measured from a sample MEMC.
Nom - Nominal values derived from analogue simulations.

Symbol	Parameter	Mes	Nom	Units	Note
IDD	Supply current			mA	
|Isc|	Output short circuit current	>25		mA	1
|Ilu|	D.C. latch-up current	300		mA	2
|Iin|	input leakage current		10	uA	
Vohc	output HIGH voltage		4.2	V	3,9
Vohioc	output HIGH voltage		3.0	V	4,11
Volc	output LOW voltage		0.3	V	3,10
Volioc	output LOW voltage		0.6	V	4,12
Vold	output LOW voltage		0.2	V	5,12
Vihct	input HIGH voltage threshold		2.8	V	6
Vilct	input LOW voltage threshold		2.0	V	6
Vihtt	input HIGH voltage threshold		2.1	V	7
Viltt	input LOW voltage threshold		1.4	V	7
Vihst	input rising voltage threshold	2.5 2.8 3.0		V V V	8,13 8,14 8,15
Vilst	input falling voltage threshold	1.5 1.7 1.9		V V V	8,13 8,14 8,15
Cin	Input capacitance	5		pF	

NOTES:

(1) Not more than one output should be shorted to either rail at any time, and for no longer than 1 second.

(2) This value represents the D.C. current that the input/output pins can tolerate before the chip latches up.

(3) OC - CMOS compatible outputs.

(4) IOCZ - bi-directional 3-state outputs.

(5) OD - open drain outputs.

IOD - bi-directional open drain outputs.

(6) IC - CMOS compatible inputs.

IOD - bi-directional open drain inputs.

IOCZ - bi-directional 3-state inputs.

(7) IT - TTL compatible inputs.

(8) IS - Schmitt triggered inputs.

(9) Output current = 3mA

(10) Output current = -3mA

(11) Output current = 10mA

(12) Output current = -10mA

(13) With VDD = 4.5 Volts

(14) With VDD = 5.0 Volts

(15) With VDD = 5.5 Volts

12. AC Parameters

TEST CONDITIONS

The AC timing diagrams presented in this section assume that the outputs of IOC have been loaded with the capacitive loads shown in the 'Test Load' column of Table 3; these loads have been chosen as typical of the type of system in which IOC will be employed.

The output pads of IOC are CMOS drivers which exhibit a propagation delay that increases linearly with the increase in load capacitance. An 'Output derating' figure is given for each output pad, showing the approximate increase in load capacitance necessary to increase the total output time by one nanosecond.

Output Signal	Test Load (pF)	Output derating (pF/ns)	Note
D[0:7]	200	8	
$\overline{SEXT}$, $\overline{WBE}$ $\overline{RE}$, $\overline{RE}$, $\overline{RBE}$ KOUT, BAUD CLK8, CLK2 $\overline{S[1:7]}$	20	5	
C[0:5], $\overline{RST}$	20	5	1
$\overline{IRQ}$, $\overline{FIQ}$ $\overline{IOGT}$, $\overline{BL}$	20	5	1

Table 3: AC test loads

NOTES:

(1) With 3K3 resistor to VDD

KEY TO TIMING TABLES

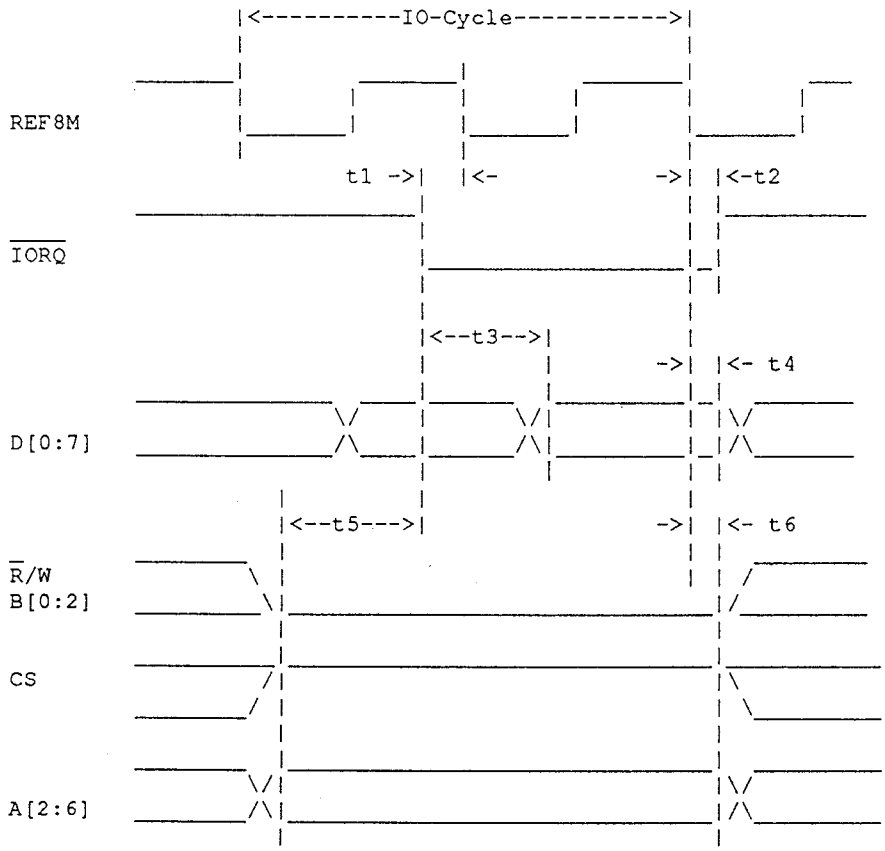
Sym - Symbol used in the timing diagrams.

Mes - Times measured in a sample ARM/MEMC/VIDC/IOC system running at 8MHz.

Nom - Nominal times.

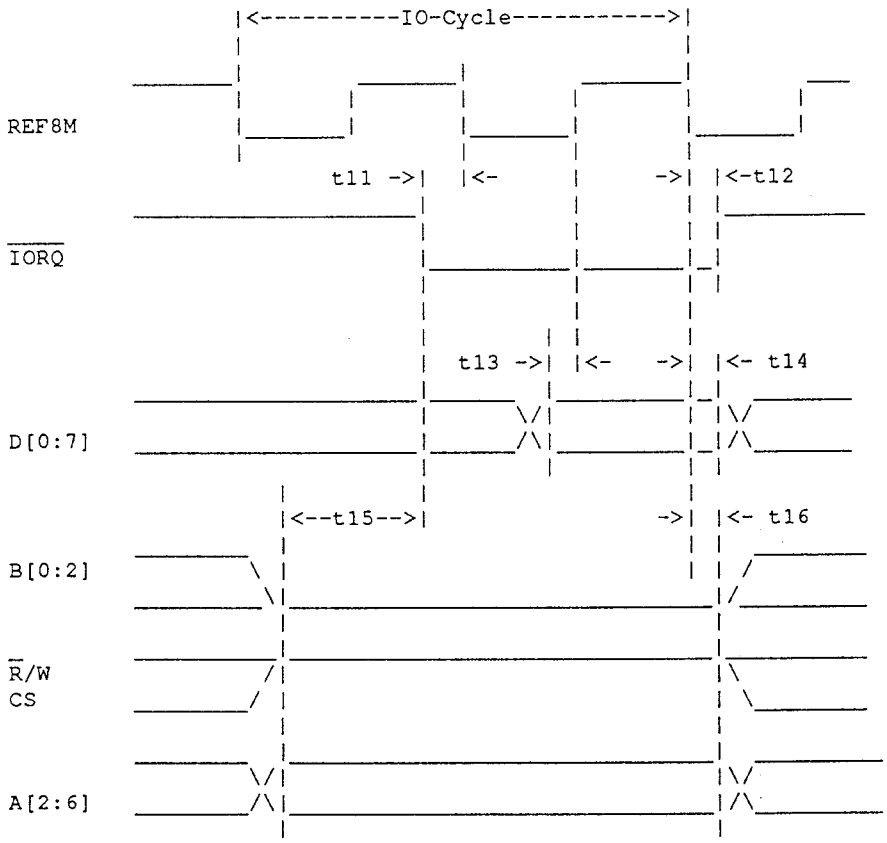
Lim - Times required to meet ARM/MEMC/VIDC/IOC system specifications.

12.1 Internal Register Read Timings



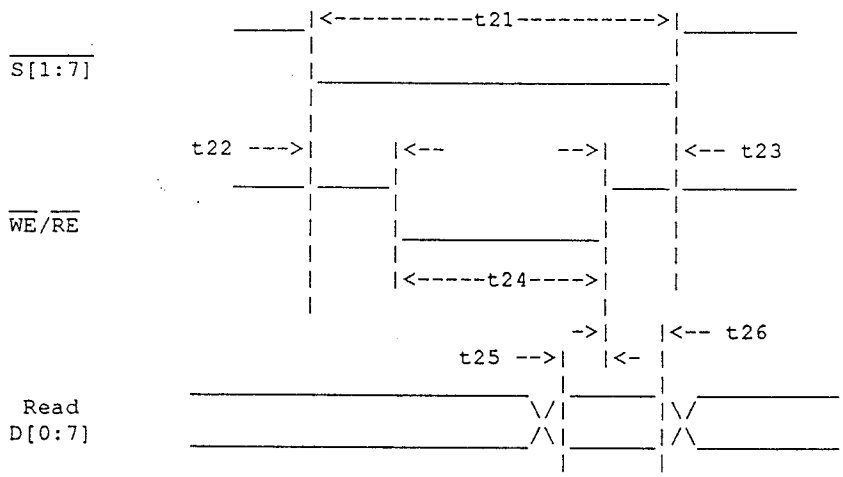
Sym	Parameter	Mes	Nom	Lim	Units	Note
t1	$\overline{\text{IORQ}}$ to REF8M set up	50		>30	ns	
t2	$\overline{\text{IORQ}}$ to REF8M hold	0	0		ns	
t3	$\overline{\text{IORQ}}$ to data valid		120		ns	
t4	data hold		0		ns	
t5	B[0:2],$\overline{\text{R}}$/W,CS,A[2:6] setup	50	50		ns	
t6	B[0:2],$\overline{\text{R}}$/W,CS,A[2:6] hold	20	10		ns	

12.2 Internal Register Write Timings



Sym	Parameter	Mes	Nom	Lim	Units	Note
t11	IORQ to REF8M set up	50		>30	ns	
t12	IORQ to REF8M hold	0	0		ns	
t13	data setup		20		ns	
t14	data hold		10		ns	
t15	B[0:2],R/W,CS,A[2:6] setup	50	50		ns	
t16	B[0:2],R/W,CS,A[2:6] hold	20	10		ns	

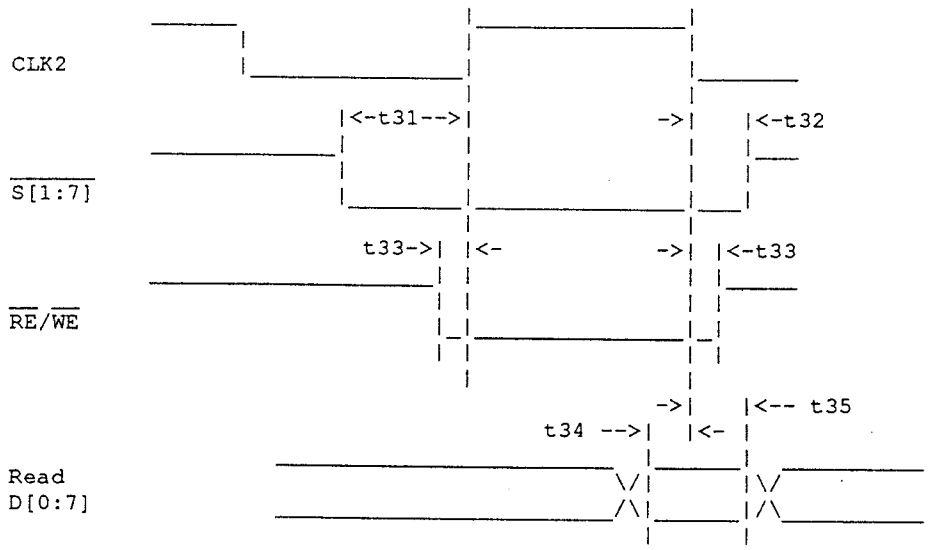
12.3 General Timing For Cycle Types 0, 1 and 2



Sym	Parameter	Mes	Nom	Lim	Units	Note
t21	$\overline{S[1:7]}$ width TYPE 0		625		ns	
t21	$\overline{S[1:7]}$ width TYPE 1		500		ns	
t21	$\overline{S[1:7]}$ width TYPE 2		375		ns	
t22	$\overline{S[1:7]}$ to $\overline{RE}/\overline{WE}$ TYPE 0		187		ns	
t22	$\overline{S[1:7]}$ to $\overline{RE}/\overline{WE}$ TYPE 1 and 2		62		ns	
t23	$\overline{RE}/\overline{WE}$ to S[1:7]		62		ns	
t24	$\overline{RE}/\overline{WE}$ width TYPE 0 and 1		375		ns	
t24	$\overline{RE}/\overline{WE}$ width TYPE 2		250		ns	
t25	read data setup to $\overline{RE}$		20		ns	1
t26	read data hold to $\overline{RE}$		20		ns	1

Note 1 : This assumes data latched by $\overline{BL}$

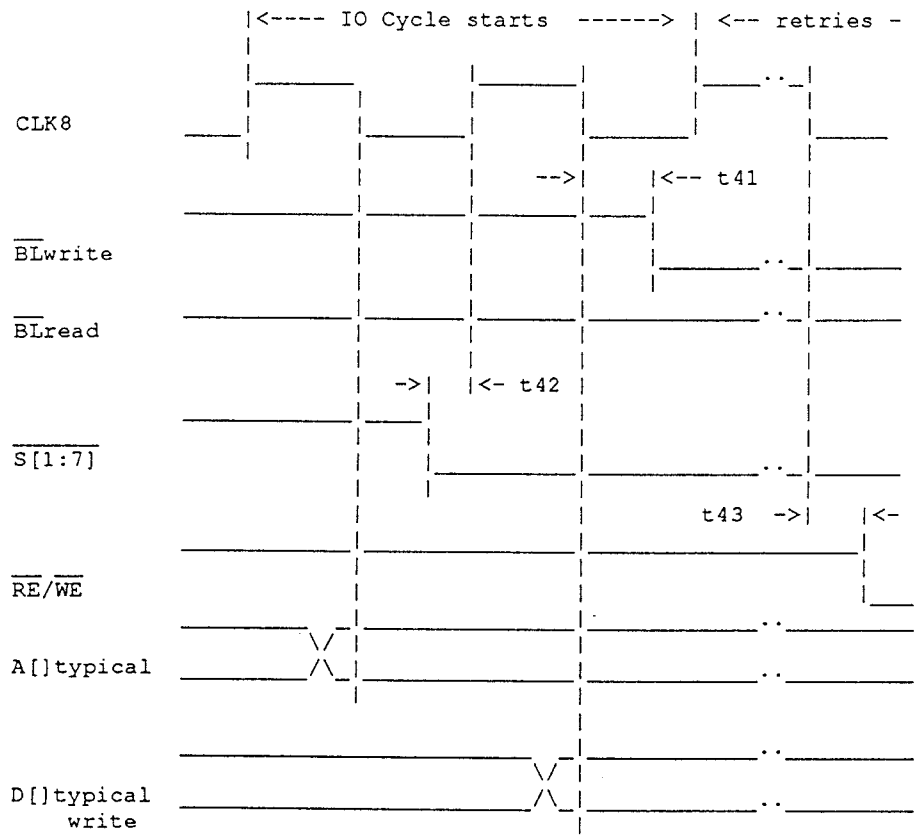
12.4 General Timings for Cycle Type 3 (Synchronous)



Sym	Parameter	Mes	Nom	Lim	Units	Note
t31	$\overline{S[1:7]}$ setup to CLK2		30		ns	
t32	$\overline{S[1:7]}$ hold to CLK2		10		ns	
t33	$\overline{RE}/\overline{WE}$ to CLK2 skew		0		ns	
t34	read data setup		20		ns	
t35	read data hold		20		ns	

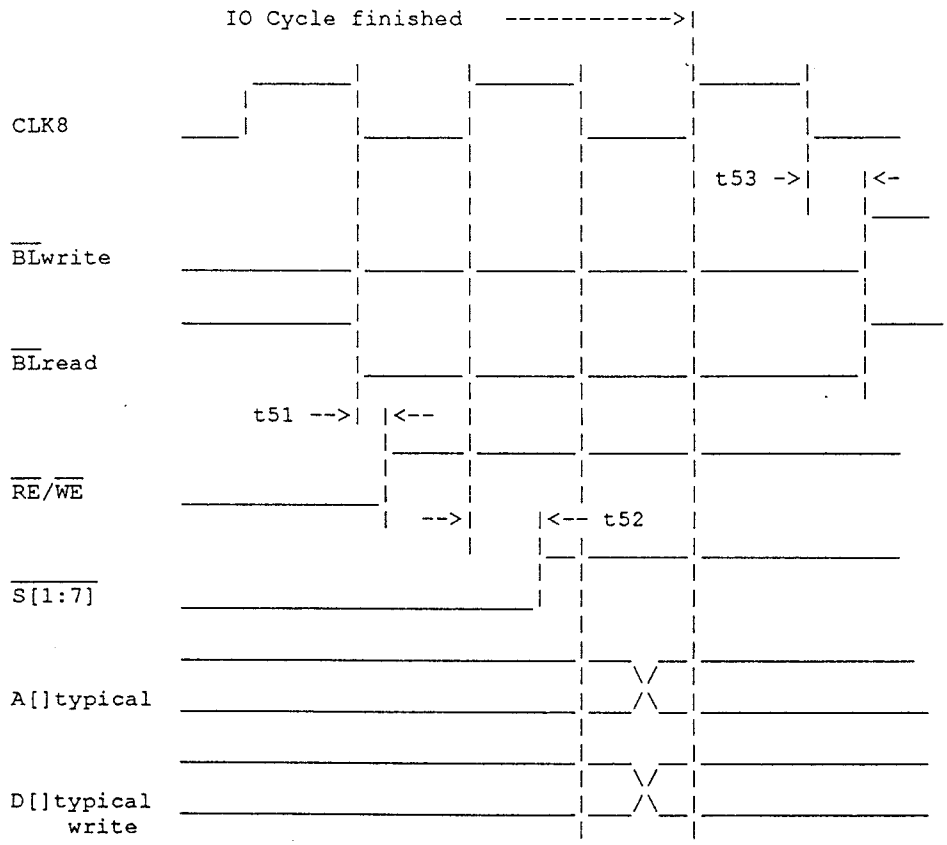
12.5 Cycle Types 0, 1, 2 Common timing

12.5.1 Cycle Start



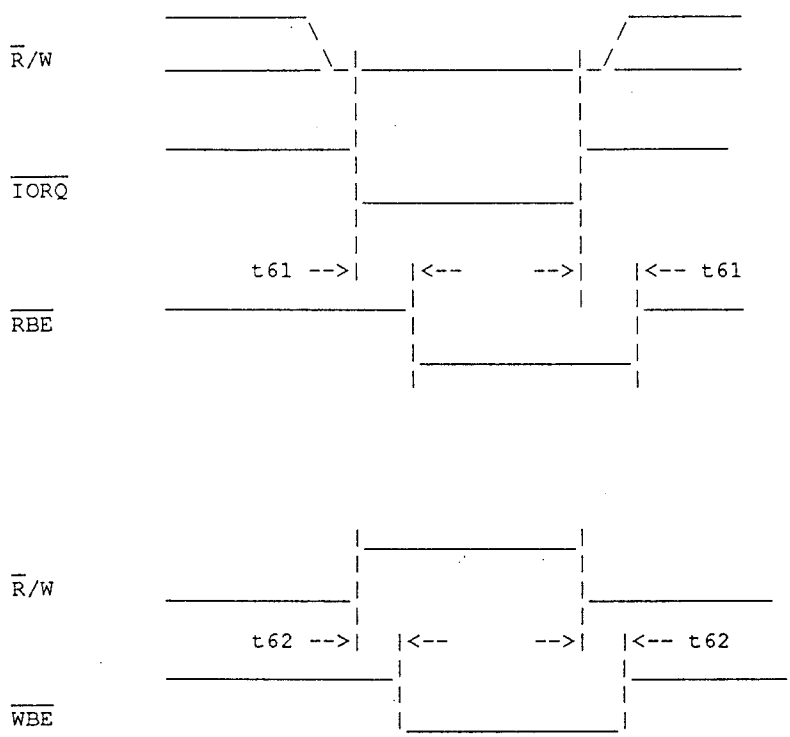
Sym	Parameter	Mes	Nom	Lim	Units	Note
t41	$\overline{BL}$ write delay		30		ns	
t42	S[1:7] setup to CLK8		10		ns	
t43	$\overline{RE}/\overline{WE}$ delay		30		ns	

12.5.2 Cycle End



Sym	Parameter	Mes	Nom	Lim	Units	Note
t51	RE/WE from CLK8 delay		30		ns	
t52	S[1:7] disable delay		30		ns	
t53	BL disable delay		30		ns	

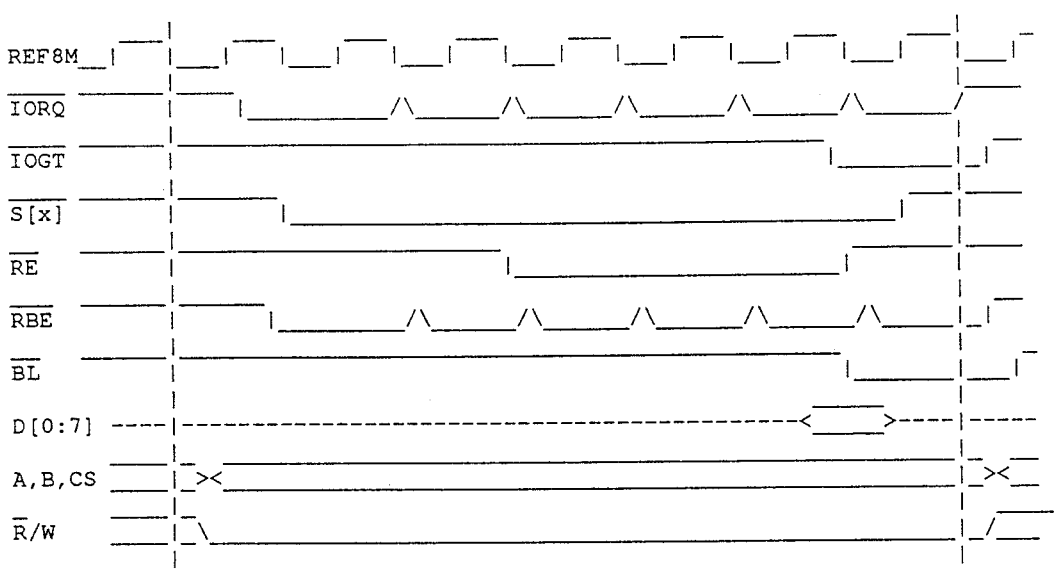
12.6 Read and Write Buffer Enables



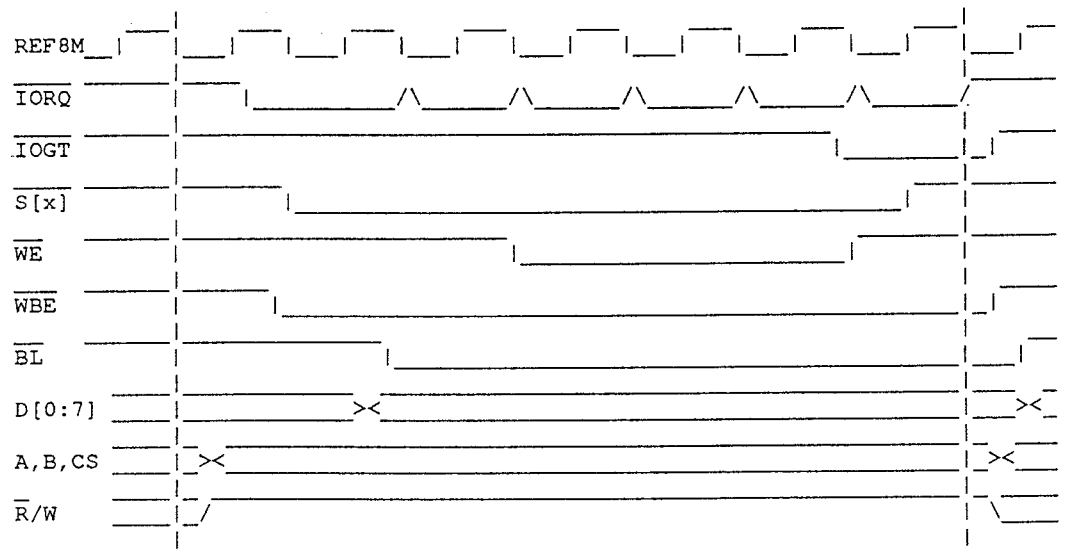
Sym	Parameter	Mes	Nom	Lim	Units	Note
t61	RBE delay from IORQ or R/W	20	50		ns	
t62	WBE delay from R/W	10	50		ns	

13. Appendix A

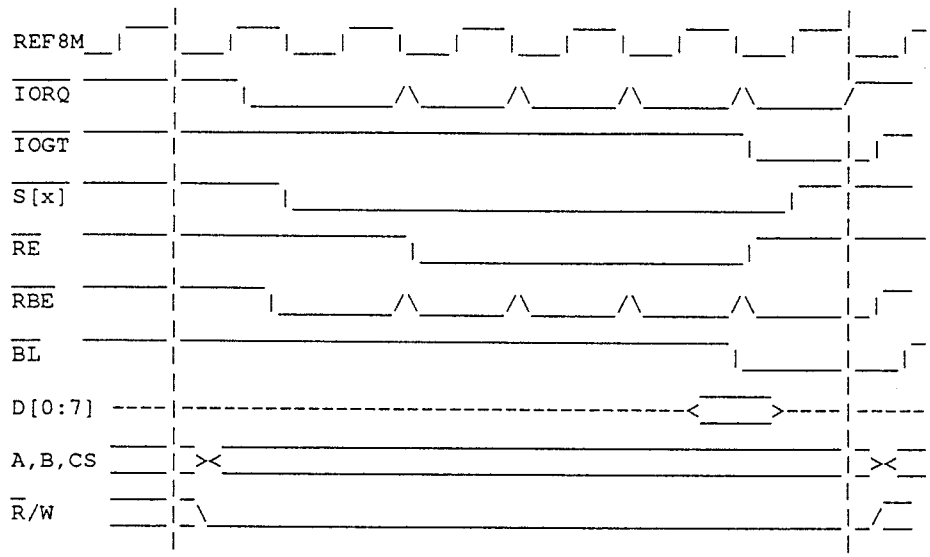
1. Cycle Type 0 Read



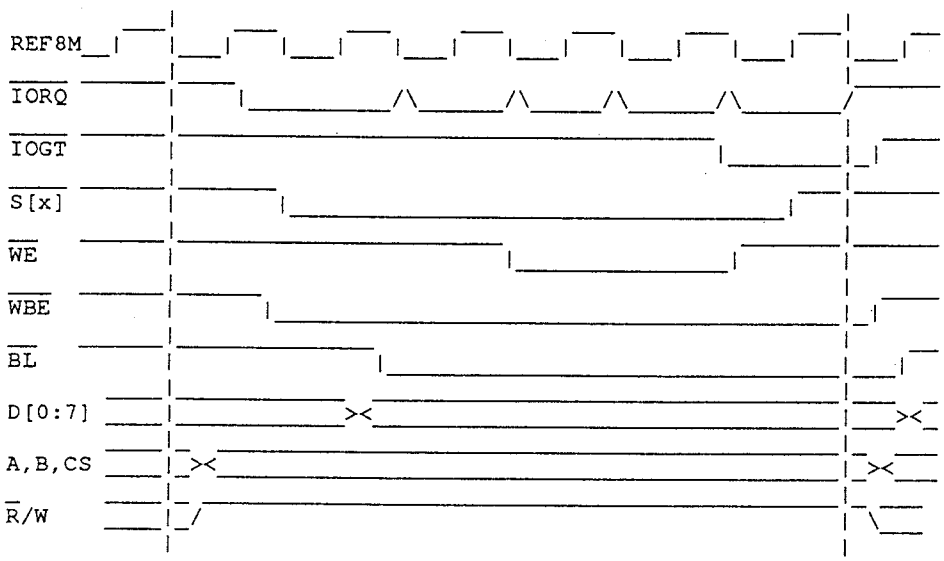
2. Cycle Type 0 Write



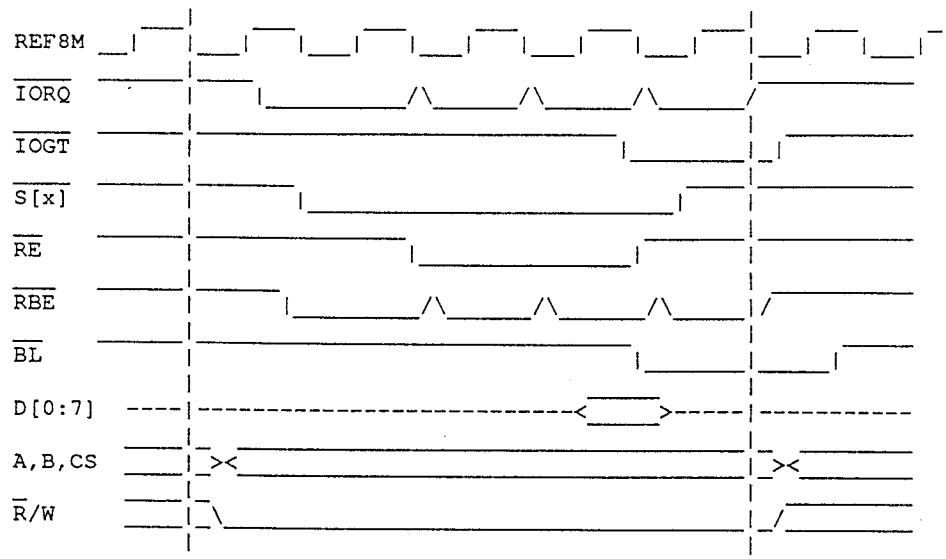
3. Cycle Type 1 Read



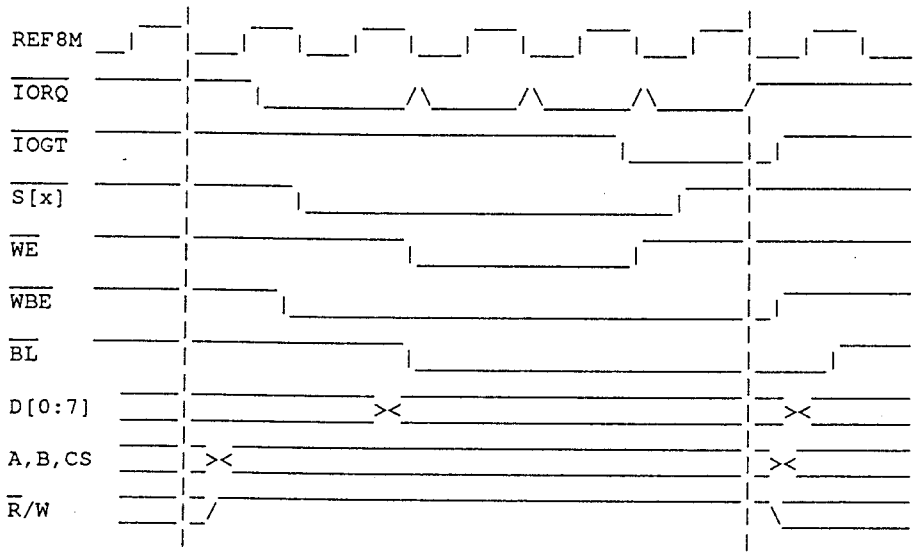
4. Cycle Type 1 Write



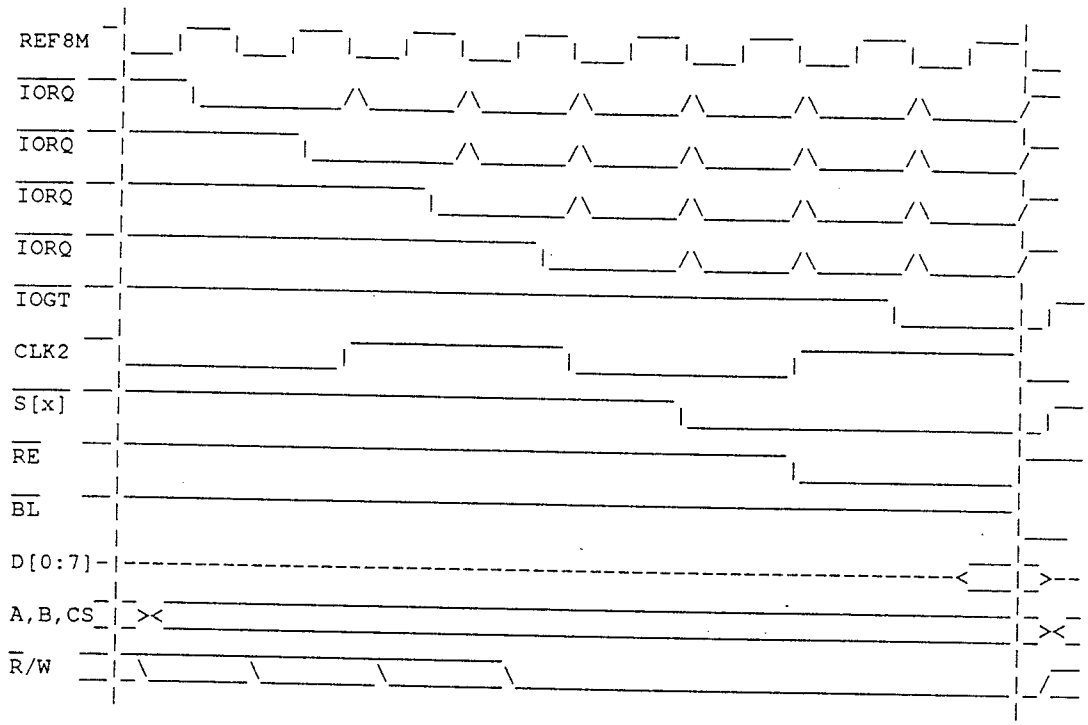
5. Cycle Type 2 Read



6. Cycle Type 2 Write

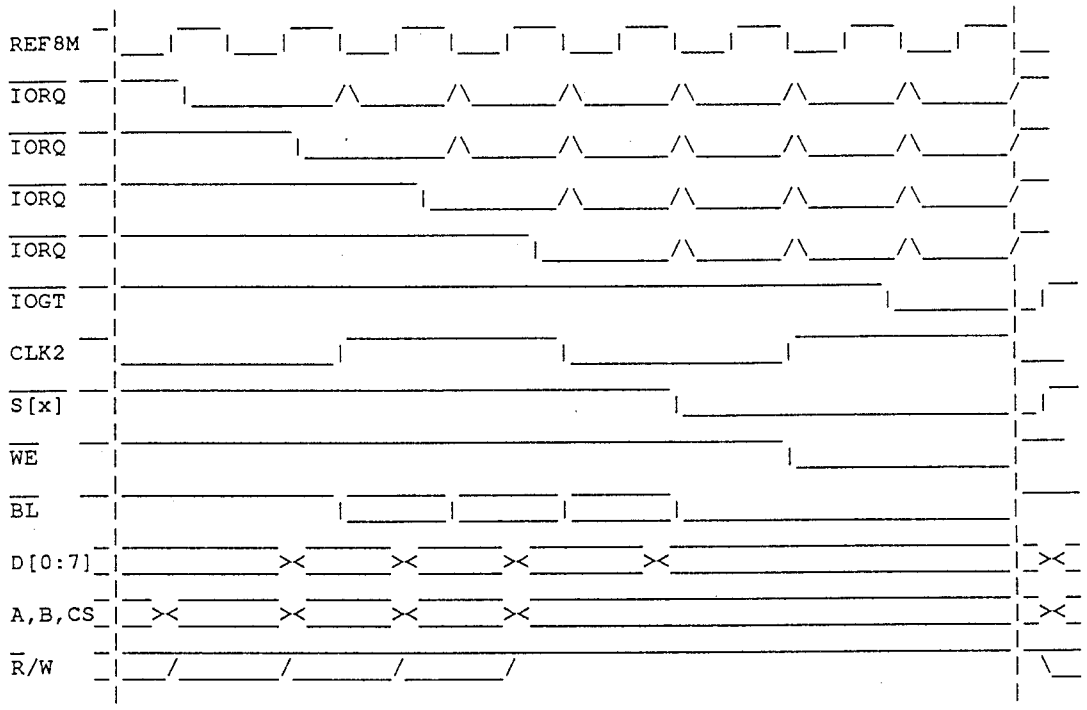


7. Cycle Type 3 Read



This shows the four different synchronisation delays represented by the four possible IORQ timings.

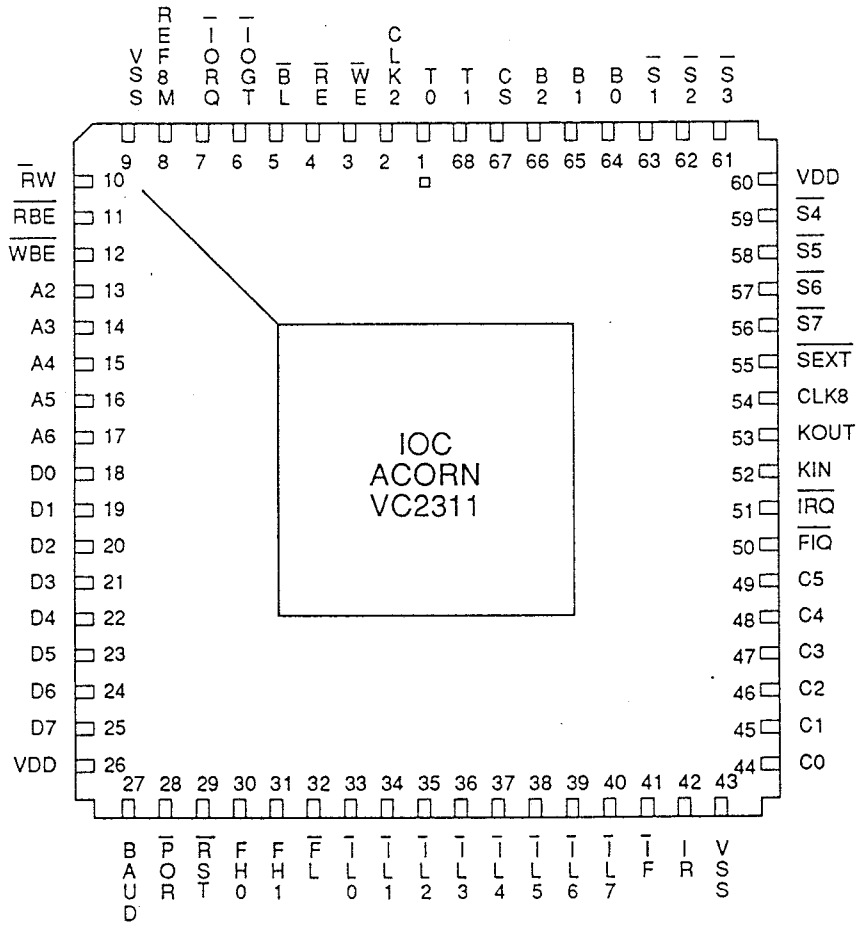
8. Cycle Type 3 Write



This shows the four different synchronisation delays represented by the four possible IORQ timings.

14. Packaging

The device is packaged in a JEDEC B ceramic leadless chip carrier, or a JEDEC C plastic leaded chip carrier (PLCC).



Suitable sockets for the devices are:

(i) AMP 55159-1 for the ceramic leadless chip carrier.

(ii) Burndy QILE68P-410T for the plastic leaded chip carrier (PLCC).